FIG. 1

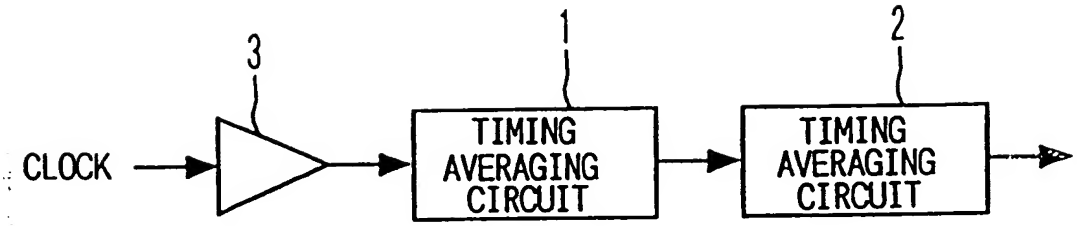


FIG. 2

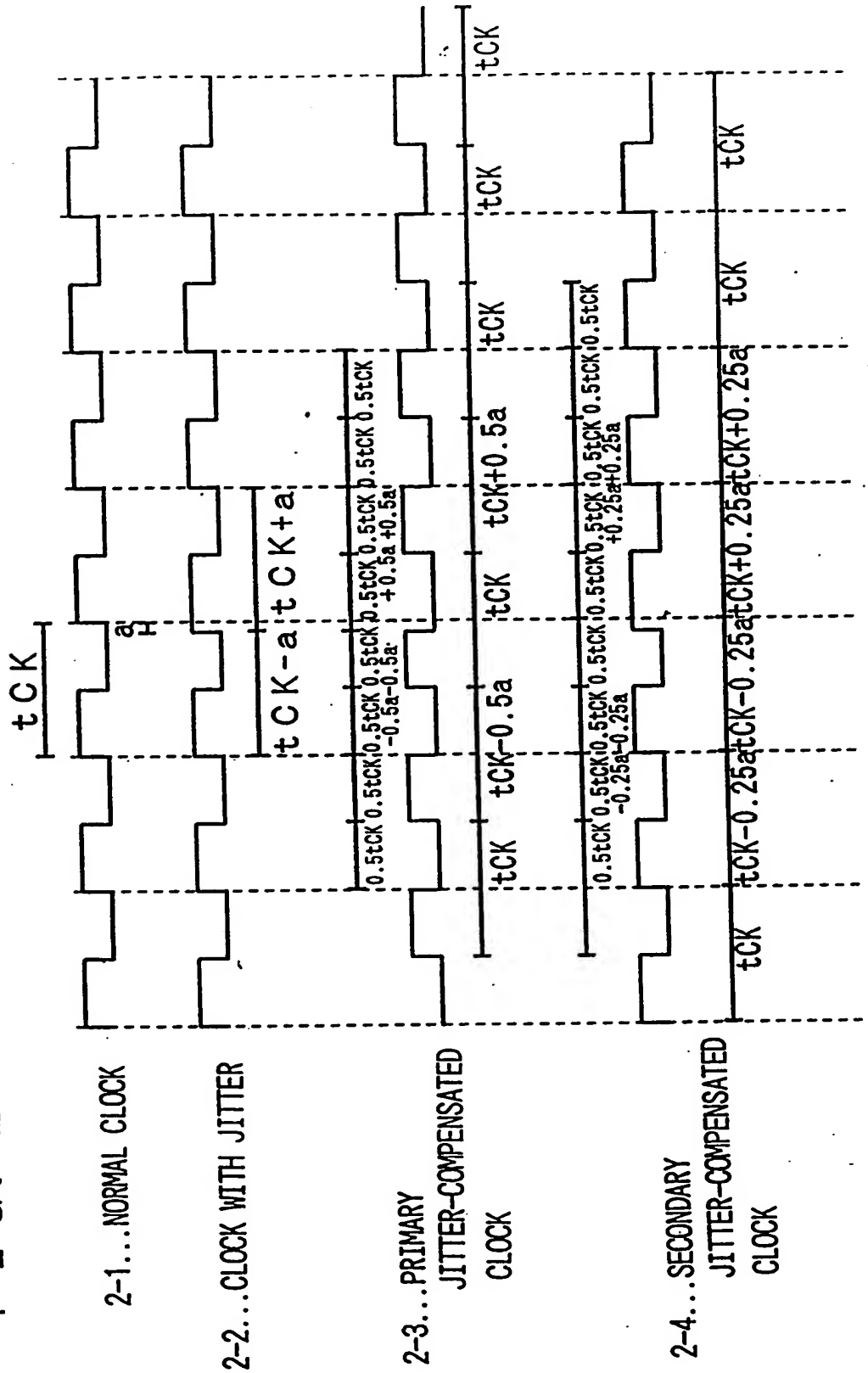

tCK
a'
H
tCK-a
tCK+a
0.5tCK 0.5tCK
-0.5a -0.5a'
0.5tCK 0.5tCK
+0.5a +0.5a'
tCK
tCK-0.5a
tCK
tCK+0.5a
0.5tCK 0.5tCK
-0.25a -0.25a
0.5tCK 0.5tCK
+0.25a +0.25a
tCK
tCK-0.25a
tCK
tCK+0.25a
2-1...NORMAL CLOCK
2-2...CLOCK WITH JITTER
2-3...PRIMARY JITTER-COMPENSATED CLOCK
2-4...SECONDARY JITTER-COMPENSATED CLOCK

FIG. 3

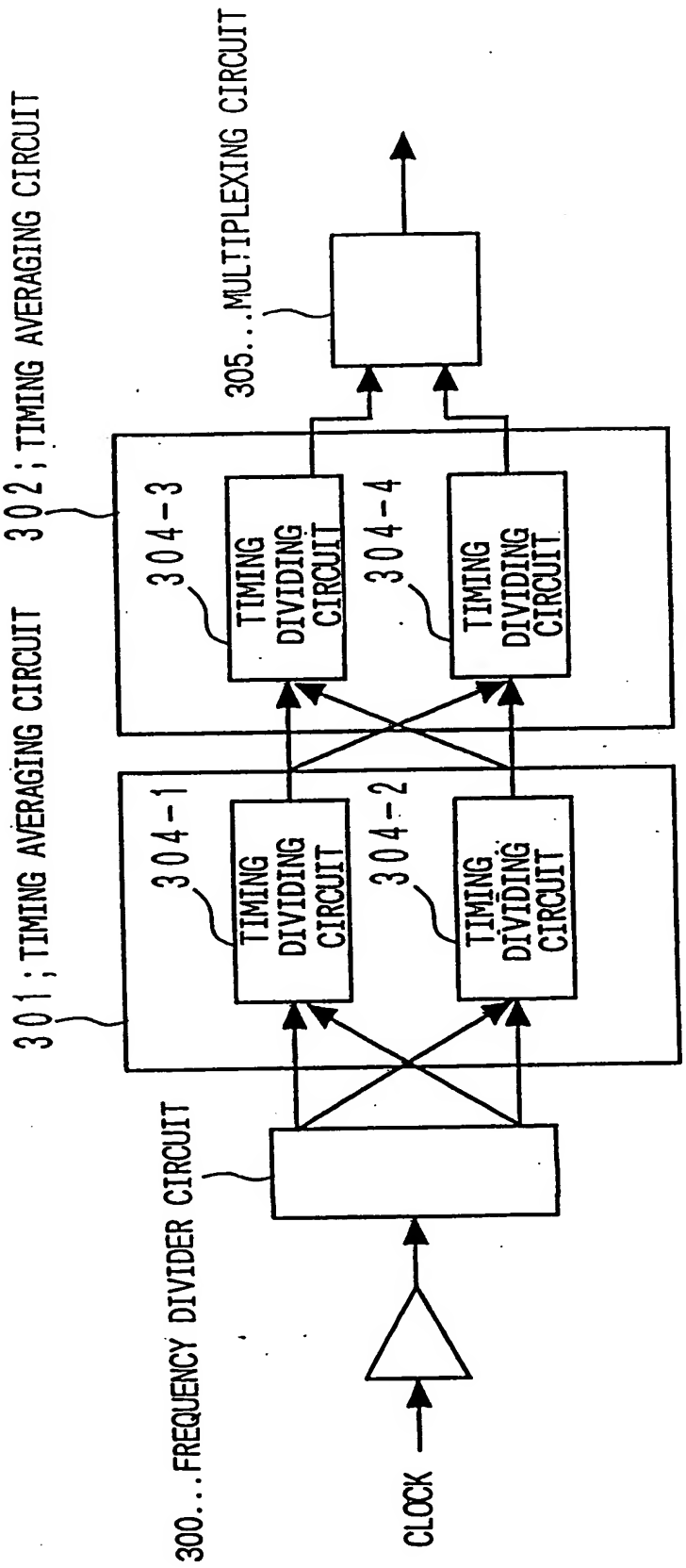

CLOCK
300...FREQUENCY DIVIDER CIRCUIT
301; TIMING AVERAGING CIRCUIT
302; TIMING AVERAGING CIRCUIT
305...MULTIPLEXING CIRCUIT
304-1
304-2
304-3
304-4
TIMING DIVIDING CIRCUIT
TIMING DIVIDING CIRCUIT
TIMING DIVIDING CIRCUIT
TIMING DIVIDING CIRCUIT

FIG. 4 (a)

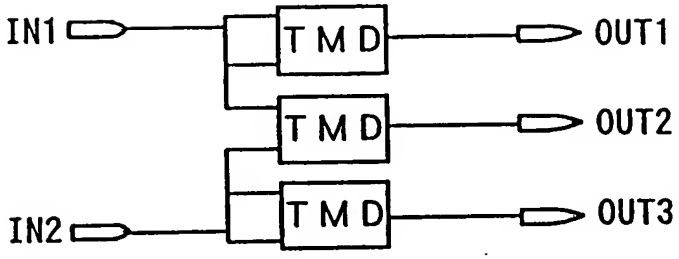


FIG. 4 (b)

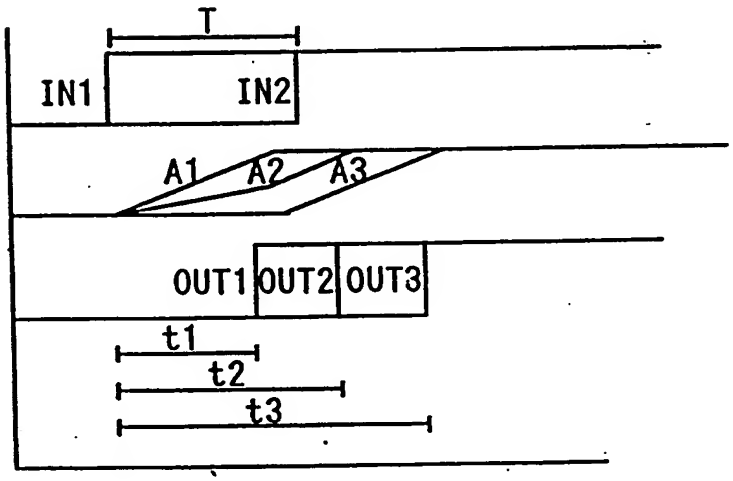


FIG. 4 (c)

$t1=CV/(i1+i2)$

$t2=T+(CV-i1T)/(i1+i2)=T+CV/(i1+i2)-i1T/(i1+i2)=T(i2/(i1+i2))+t1$

$t2=(1/2)T+t1$

$t3=T+CV/(i1+i2)=T+t1$

FIG. 5 (a)

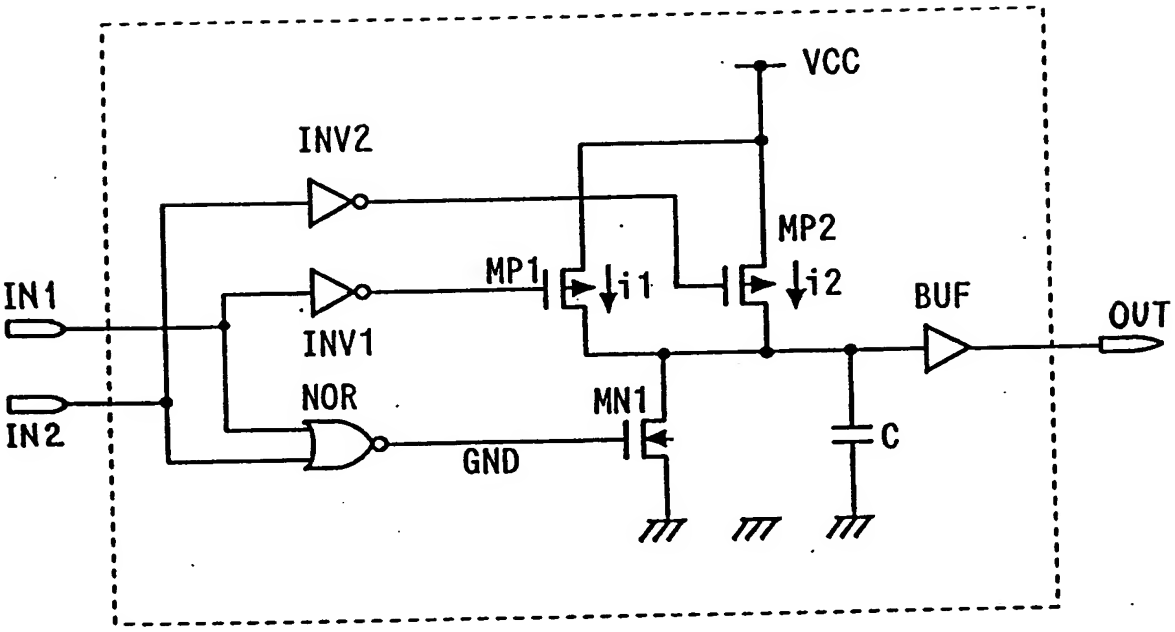
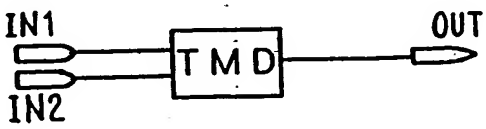

VCC
INV2
MP2
MP1
i1
i2
IN1
INV1
BUF
OUT
NOR
MN1
IN2
GND
C

FIG. 5 (b)


IN1
TMD
OUT
IN2

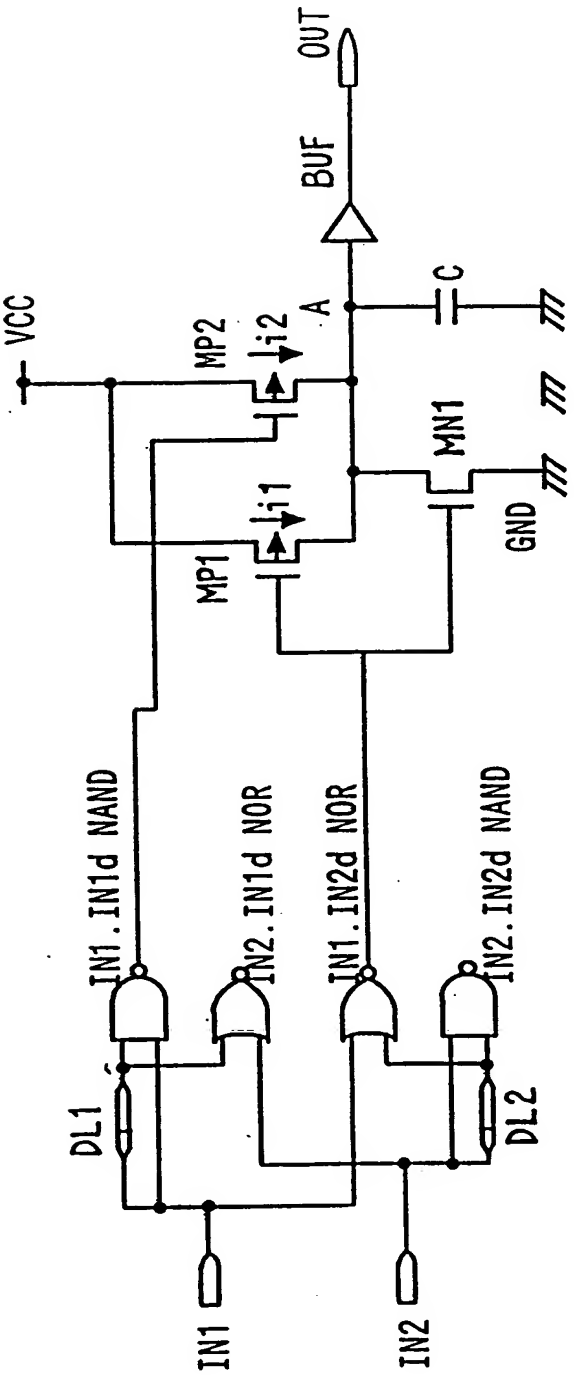

OUT
BUF
C
A
VCC
MP2
i2
MN1
i1
GND
MP1
IN1.IN1d NAND
IN2.IN1d NOR
IN1.IN2d NOR
IN2.IN2d NAND
DL1
DL2
IN1
IN2

FIG. 6

FIG. 7

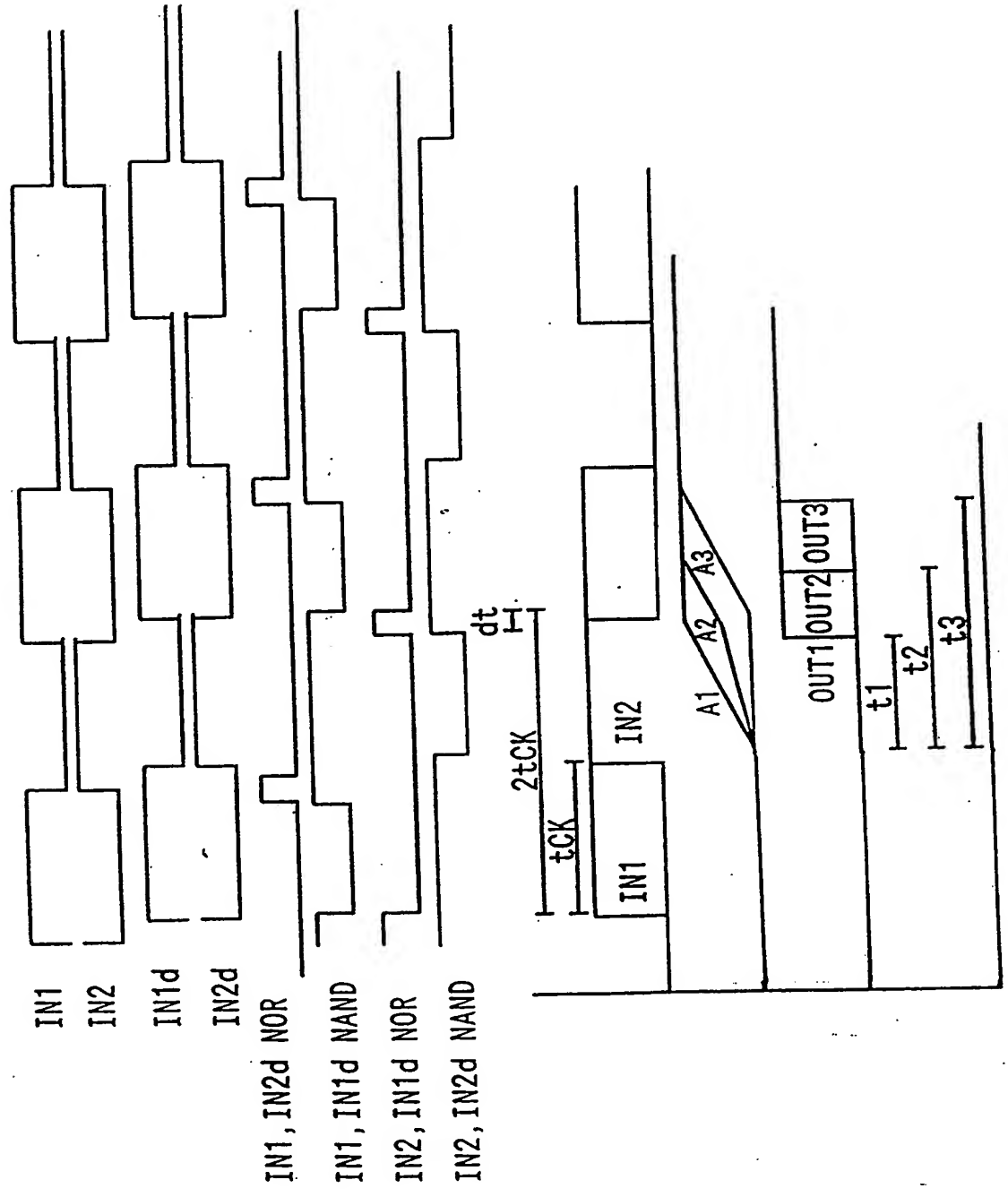

IN1
IN2
IN1d
IN2d
IN1, IN2d NOR
IN1, IN1d NAND
IN2, IN1d NOR
IN2, IN2d NAND
dt
2tCK
tCK
IN1
IN2
A1
A2
A3
OUT1
OUT2
OUT3
t1
t2
t3

FIG. 8

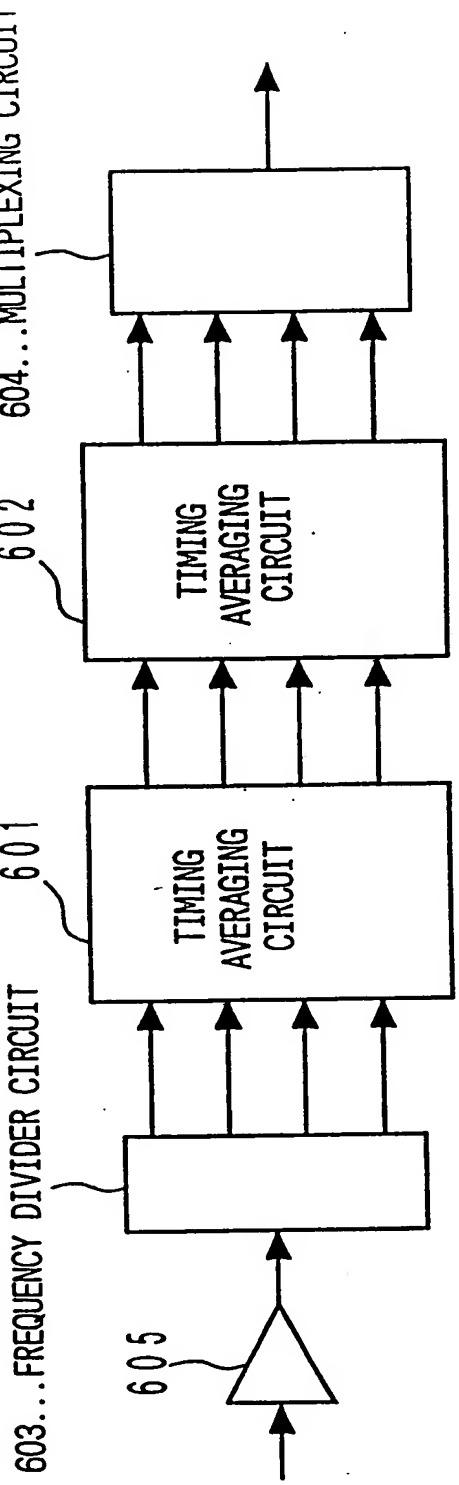
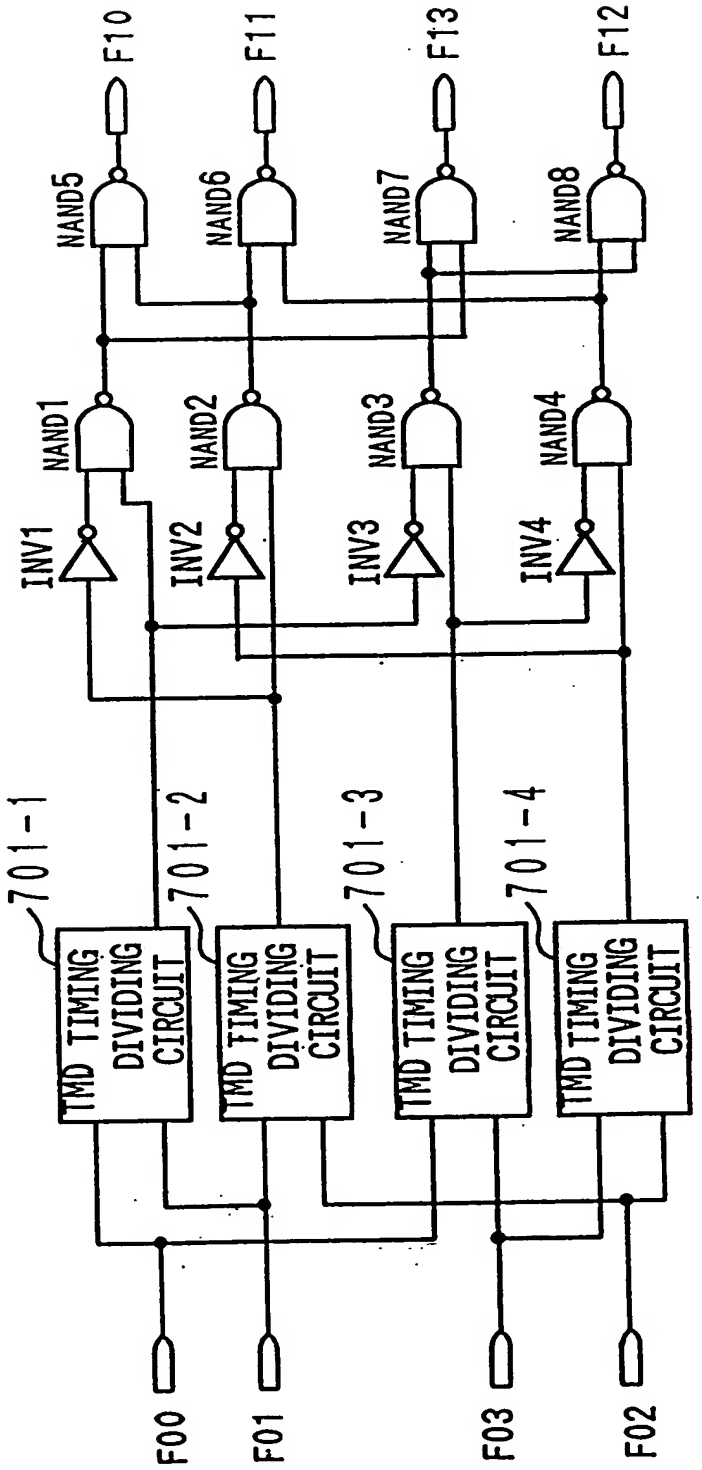

603...FREQUENCY DIVIDER CIRCUIT
605
601
TIMING AVERAGING CIRCUIT
602
TIMING AVERAGING CIRCUIT
604...MULTIPLEXING CIRCUIT

FIG. 9


F10
F11
F13
F12
NAND5
NAND6
NAND7
NAND8
NAND1
NAND2
NAND3
NAND4
INV1
INV2
INV3
INV4
701-1
701-2
701-3
701-4
TMD TIMING DIVIDING CIRCUIT
TMD TIMING DIVIDING CIRCUIT
TMD TIMING DIVIDING CIRCUIT
TMD TIMING DIVIDING CIRCUIT
F00
F01
F03
F02

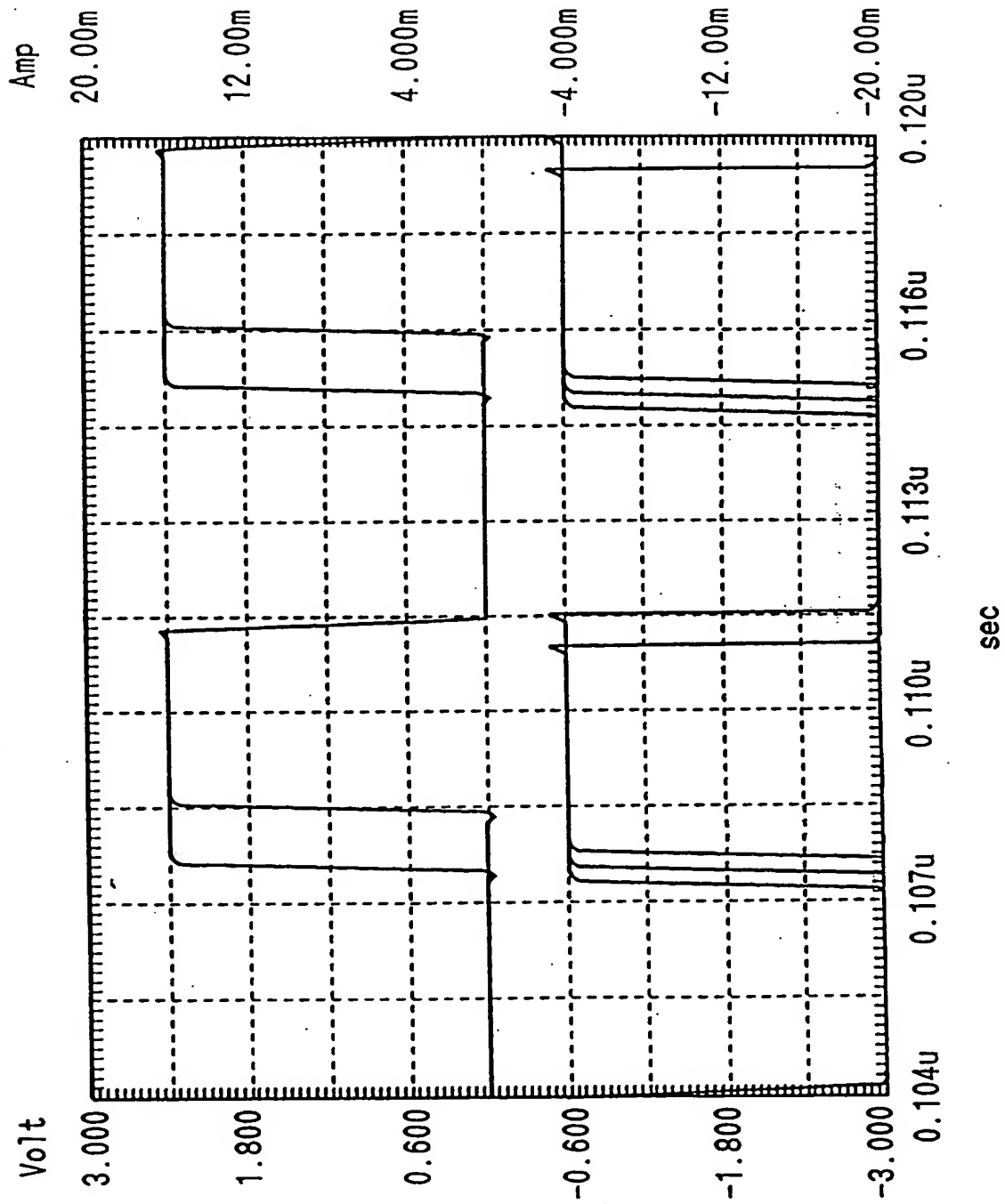

Amp
20.00m
12.00m
4.000m
-4.000m
-12.00m
-20.00m
Volt
3.000
1.800
0.600
-0.600
-1.800
-3.000
0.104u
0.107u
0.110u
0.113u
0.116u
0.120u
sec

FIG. 10

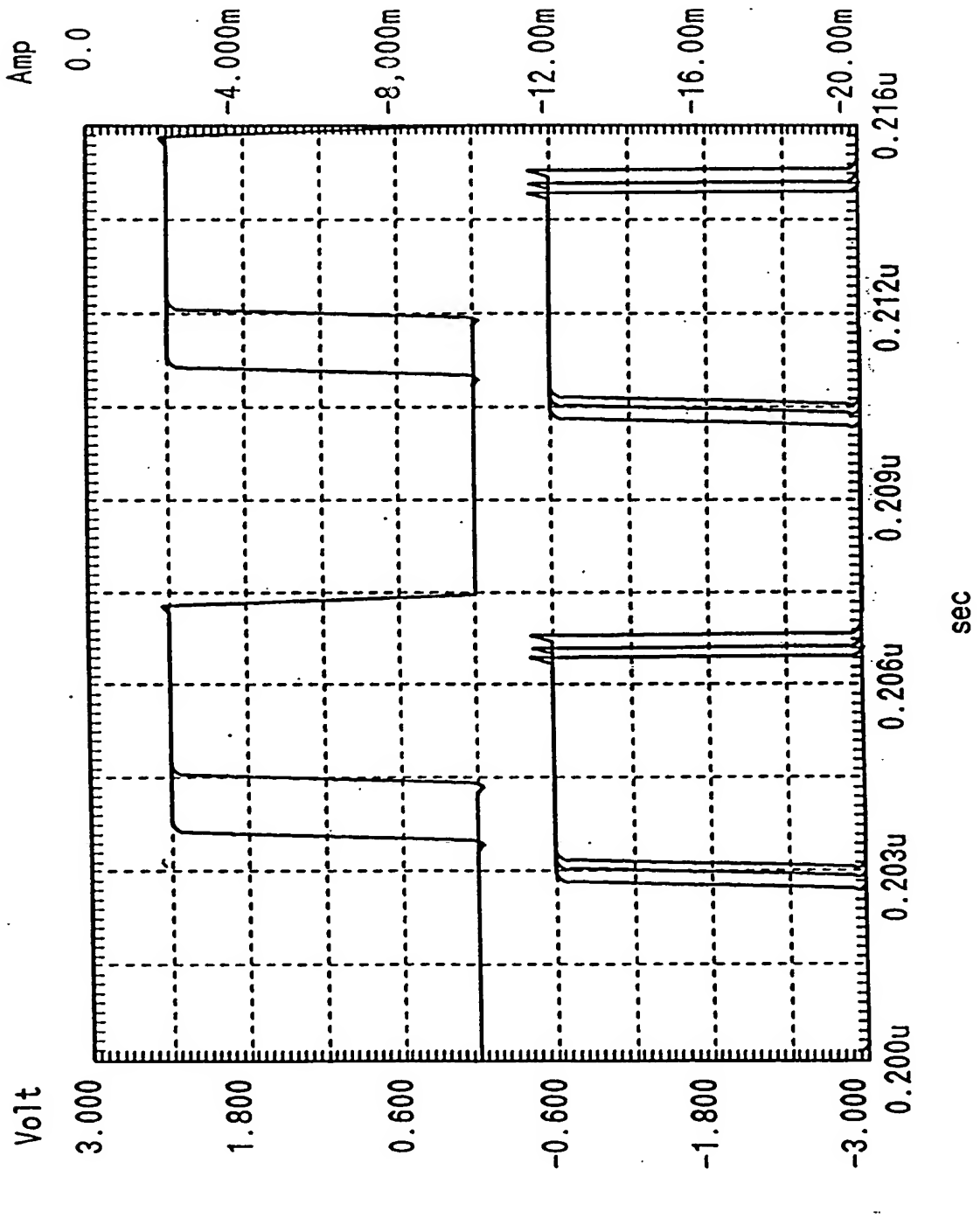

Amp
0.0
-4.000m
-8.000m
-12.00m
-16.00m
-20.00m
Volt
3.000
1.800
0.600
-0.600
-1.800
-3.000
0.200u
0.203u
0.206u
0.209u
0.212u
0.216u
sec

FIG. 11

FIG. 12

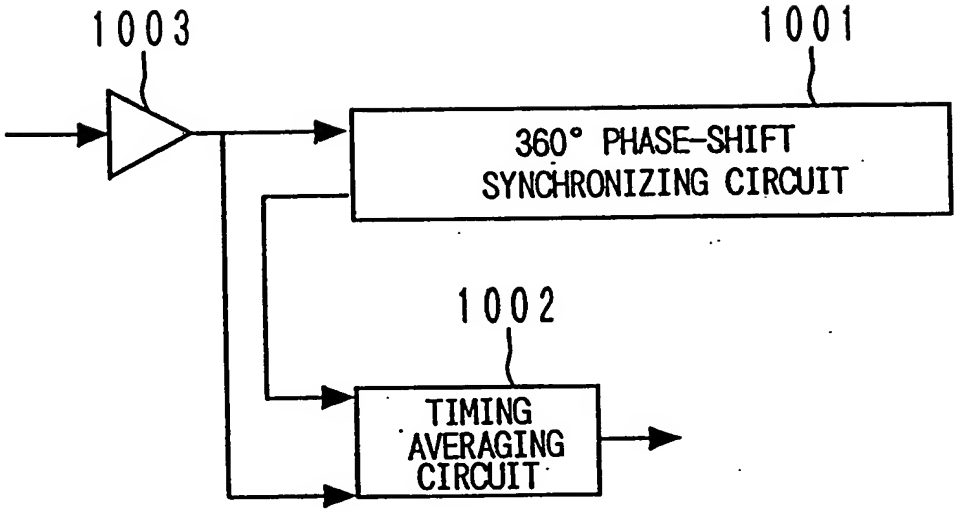

1003
1001
360° PHASE-SHIFT SYNCHRONIZING CIRCUIT
1002
TIMING AVERAGING CIRCUIT

FIG. 13

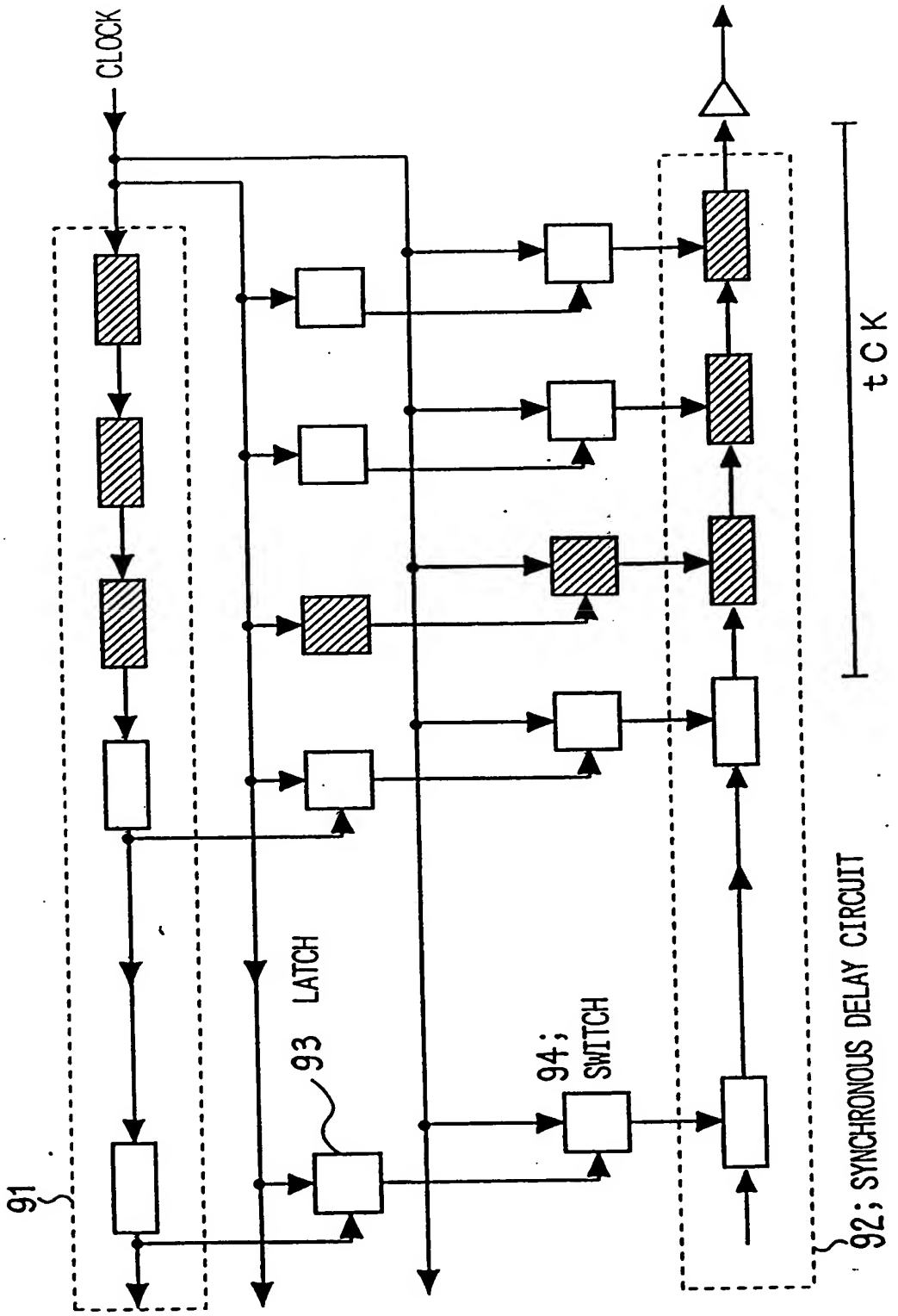

CLOCK
91
93 LATCH
94; SWITCH
92; SYNCHRONOUS DELAY CIRCUIT
tCK

FIG. 14

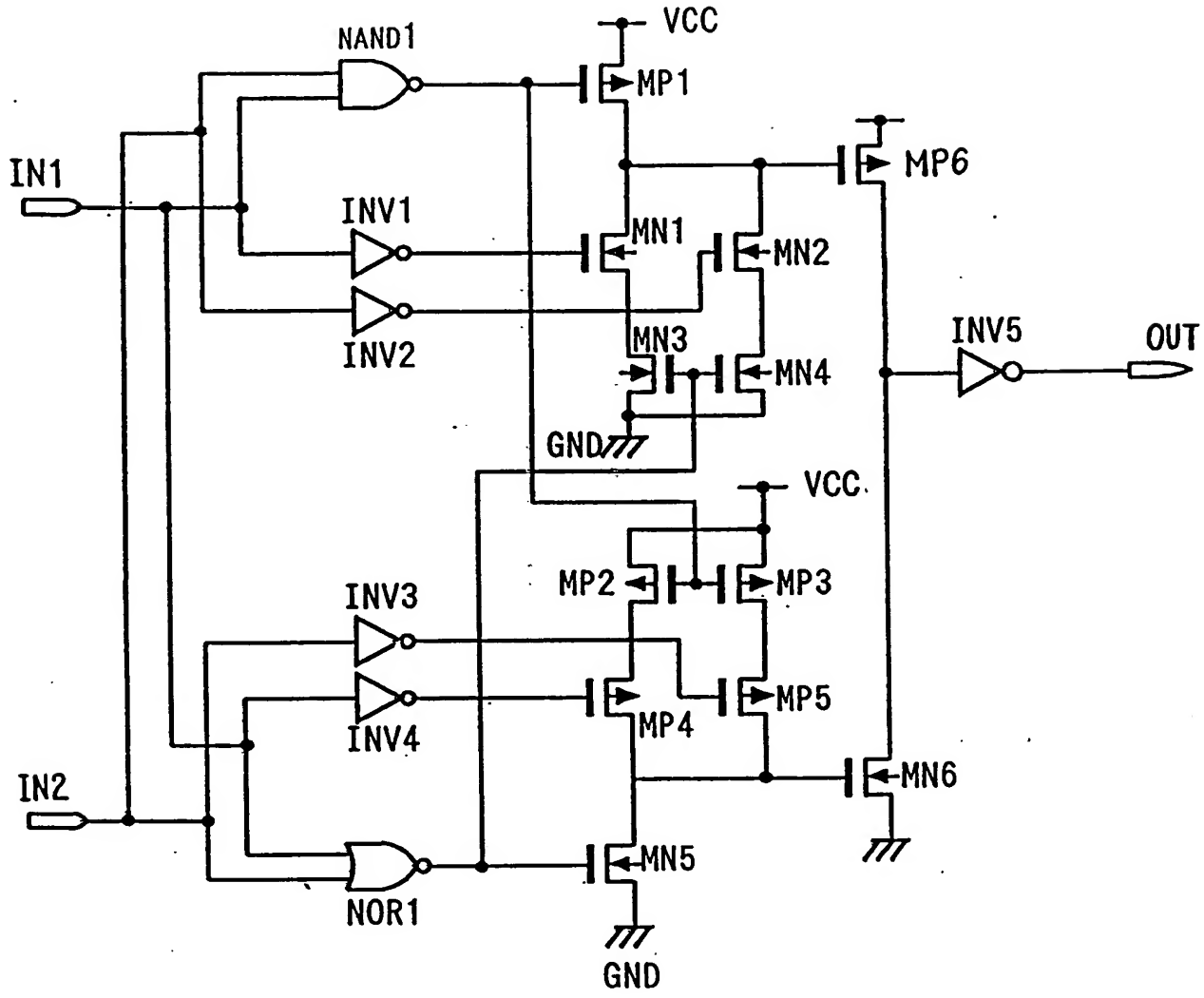

NAND1
VCC
MP1
MP6
IN1
INV1
MN1
MN2
INV2
MN3
MN4
INV5
OUT
GND
VCC
MP2
MP3
INV3
INV4
MP4
MP5
MN6
IN2
MN5
NOR1
GND

FIG. 15

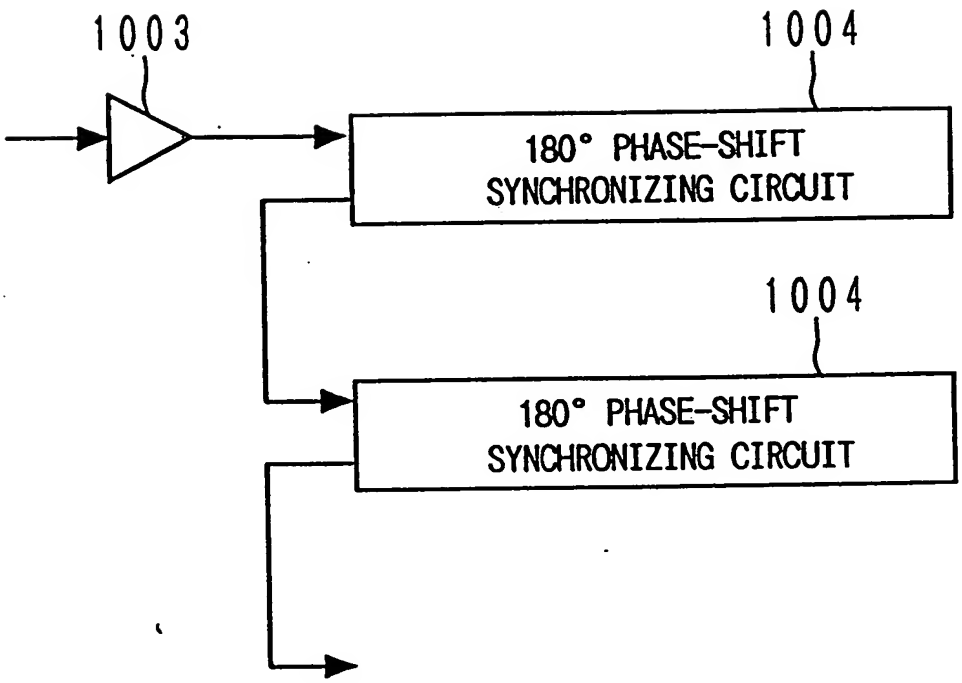

1003
1004
180° PHASE-SHIFT SYNCHRONIZING CIRCUIT
1004
180° PHASE-SHIFT SYNCHRONIZING CIRCUIT

FIG. 16

PRIOR ART

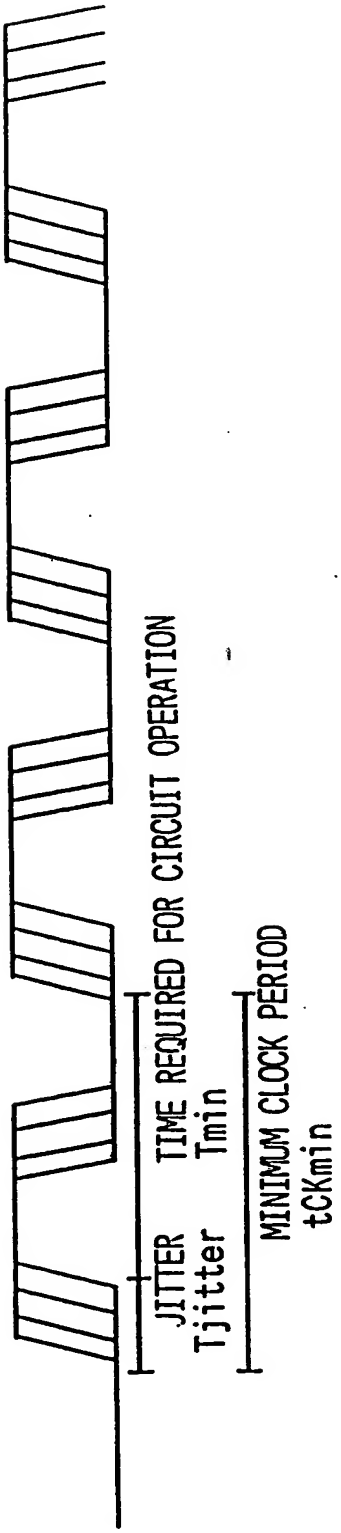


FIG. 17

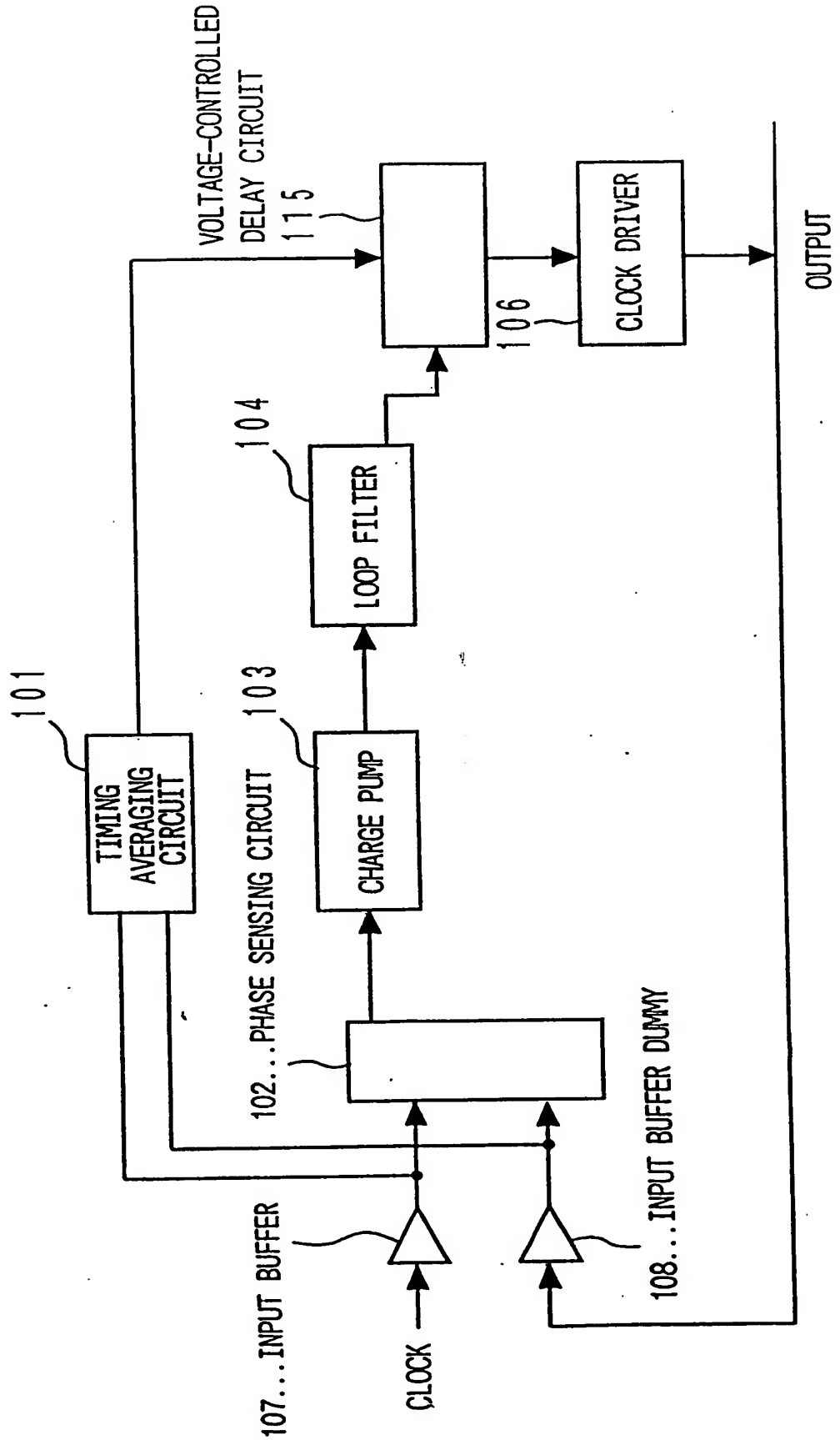

VOLTAGE-CONTROLLED DELAY CIRCUIT
115
106
CLOCK DRIVER
OUTPUT
104
LOOP FILTER
101
TIMING AVERAGING CIRCUIT
103
CHARGE PUMP
102...PHASE SENSING CIRCUIT
107...INPUT BUFFER
CLOCK
108...INPUT BUFFER DUMMY

FIG. 18

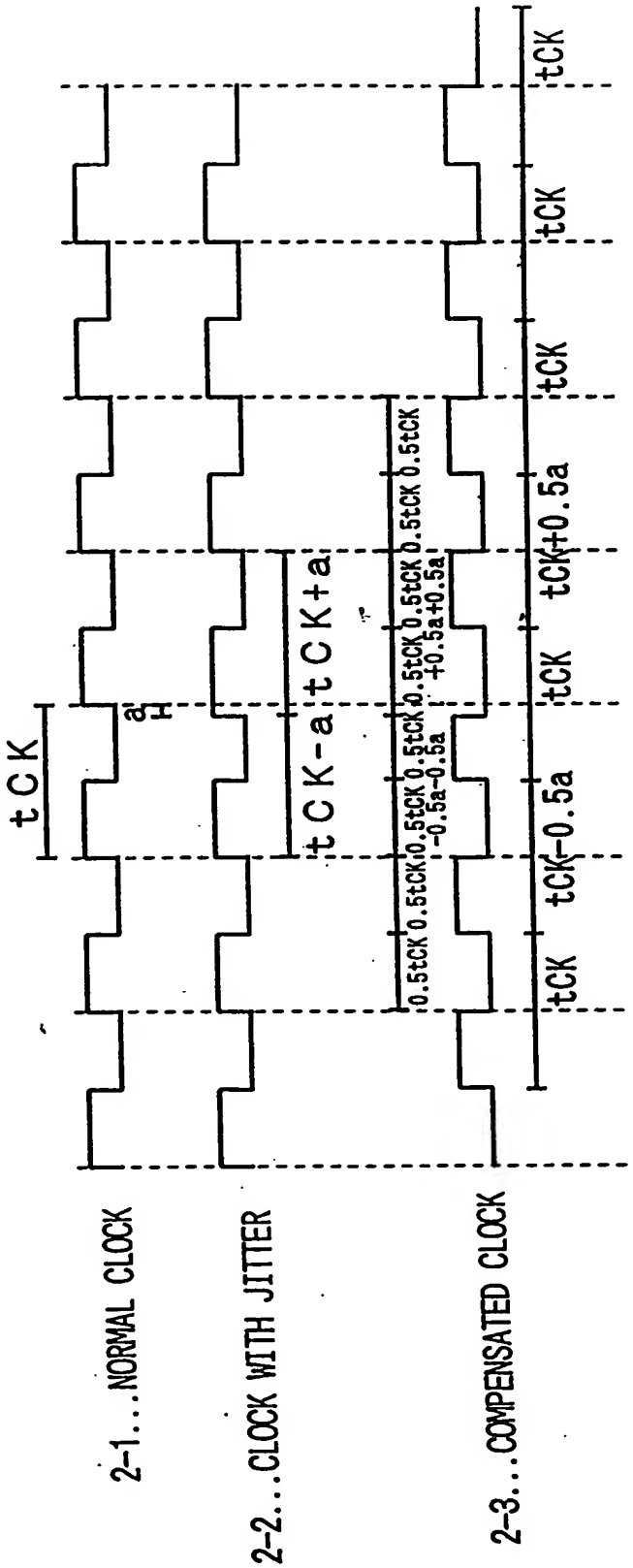

tCK
a
H
tCK-a
tCK+a
0.5tCK
0.5tCK
-0.5a
0.5tCK
0.5tCK
+0.5a
tCK
tCK
tCK
tCK-0.5a
tCK+0.5a
tCK
tCK
2-1...NORMAL CLOCK
2-2...CLOCK WITH JITTER
2-3...COMPENSATED CLOCK

FIG. 19

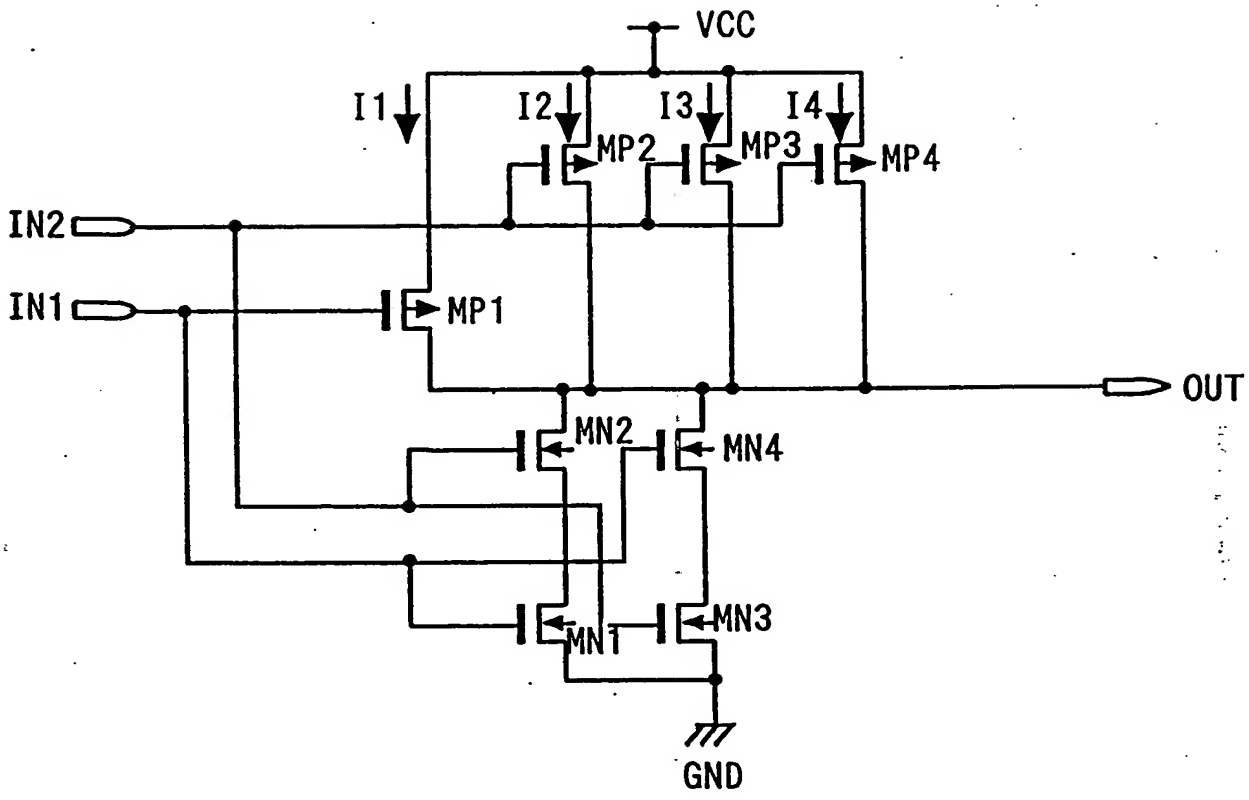
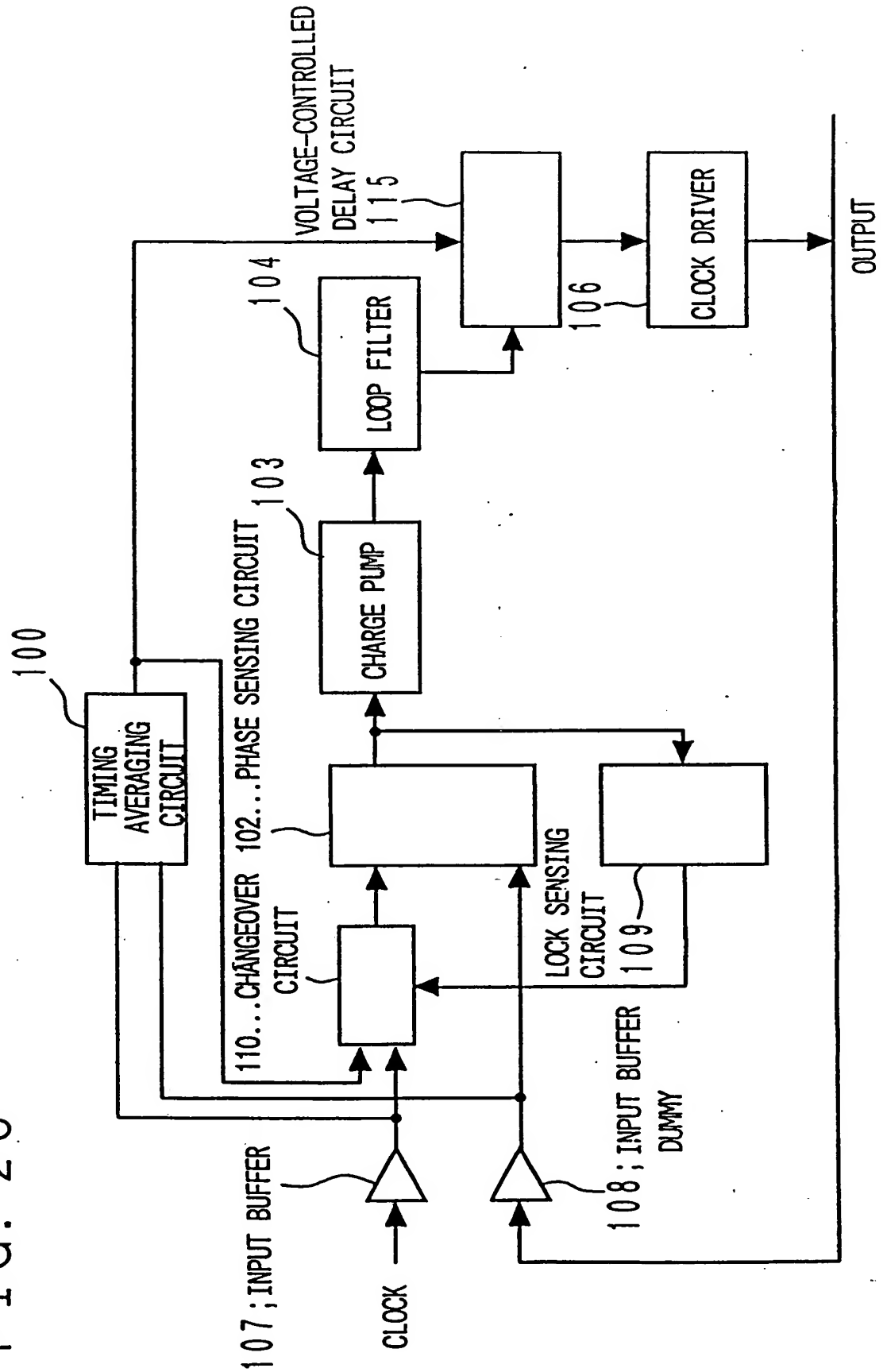


FIG. 20


100
TIMING AVERAGING CIRCUIT
110...CHANGEOVER CIRCUIT
102...PHASE SENSING CIRCUIT
103
CHARGE PUMP
104
LOOP FILTER
VOLTAGE-CONTROLLED DELAY CIRCUIT 115
106
CLOCK DRIVER
OUTPUT
LOCK SENSING CIRCUIT 109
107; INPUT BUFFER
108; INPUT BUFFER DUMMY
CLOCK

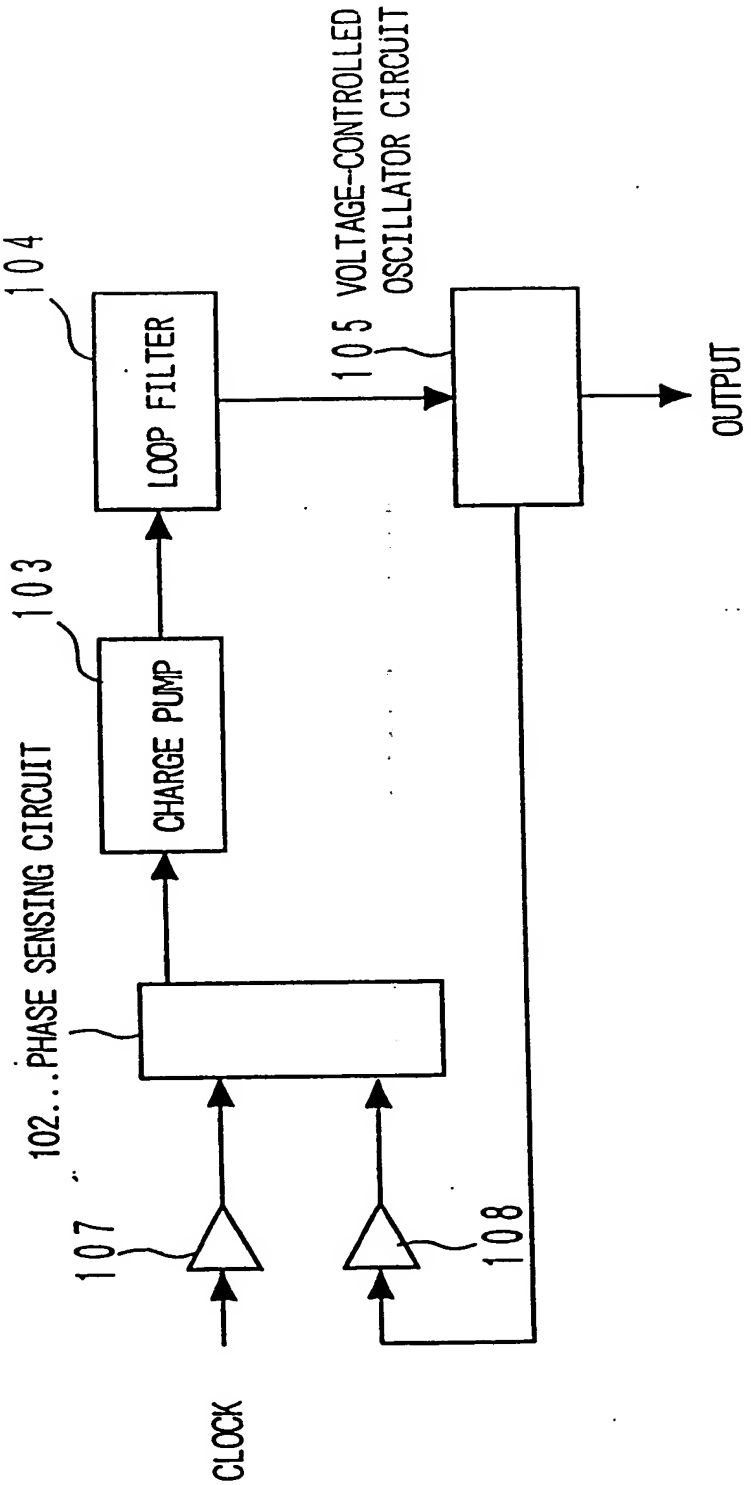


FIG. 21

RELATED ART

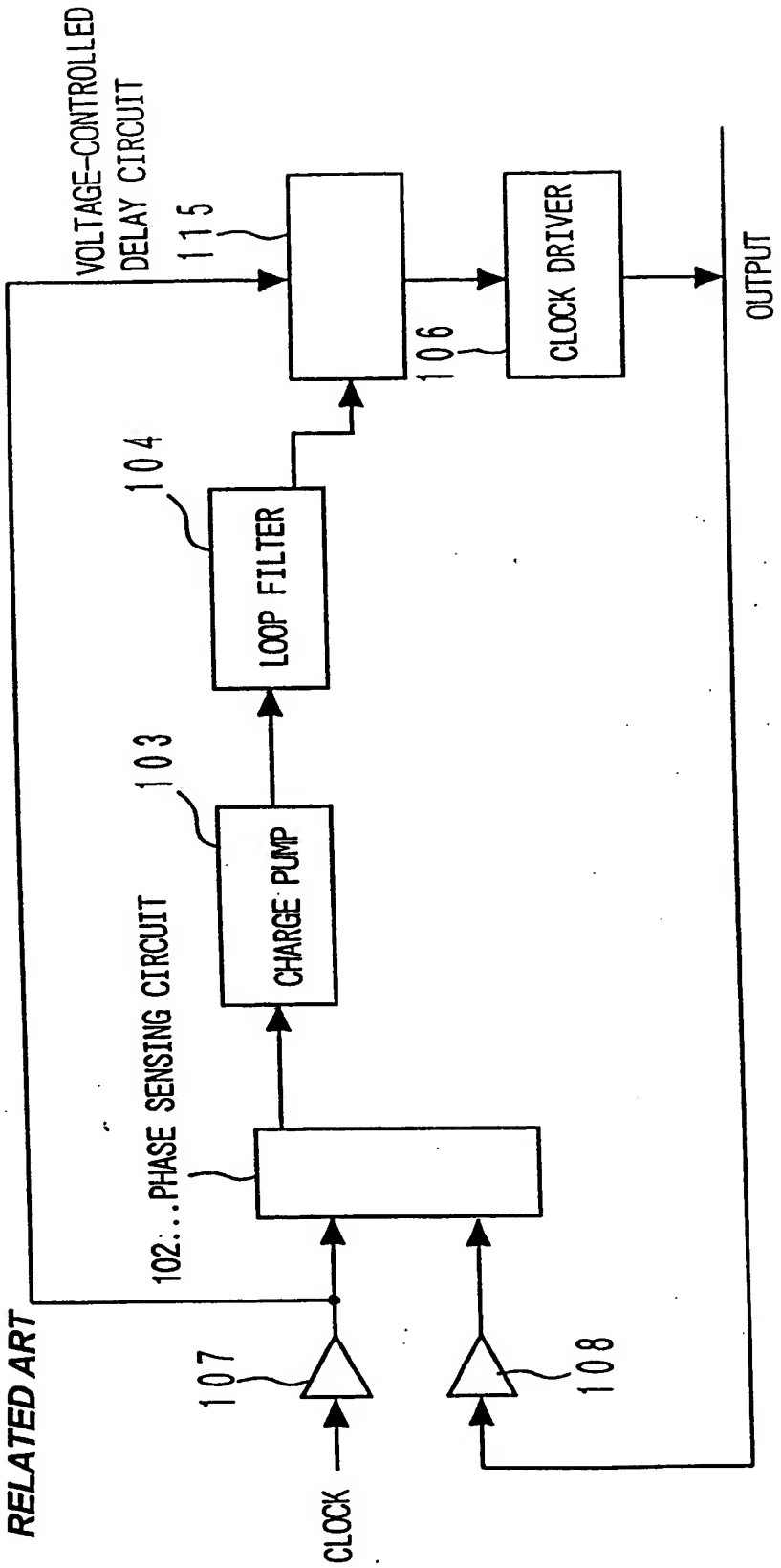


FIG. 22
RELATED ART

FIG. 23 (a)

RELATED ART

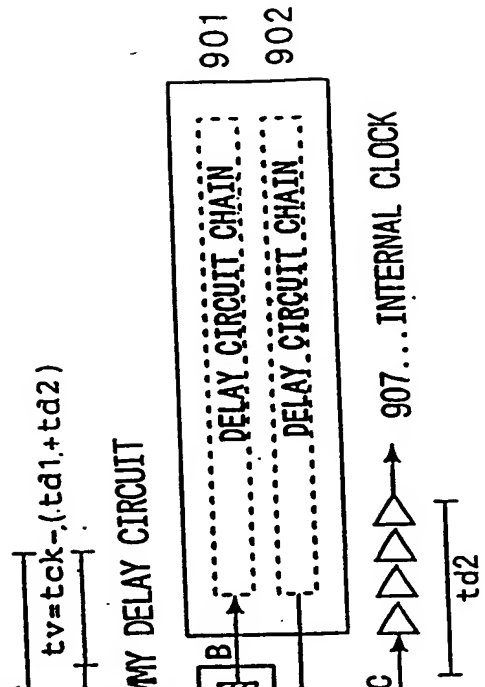
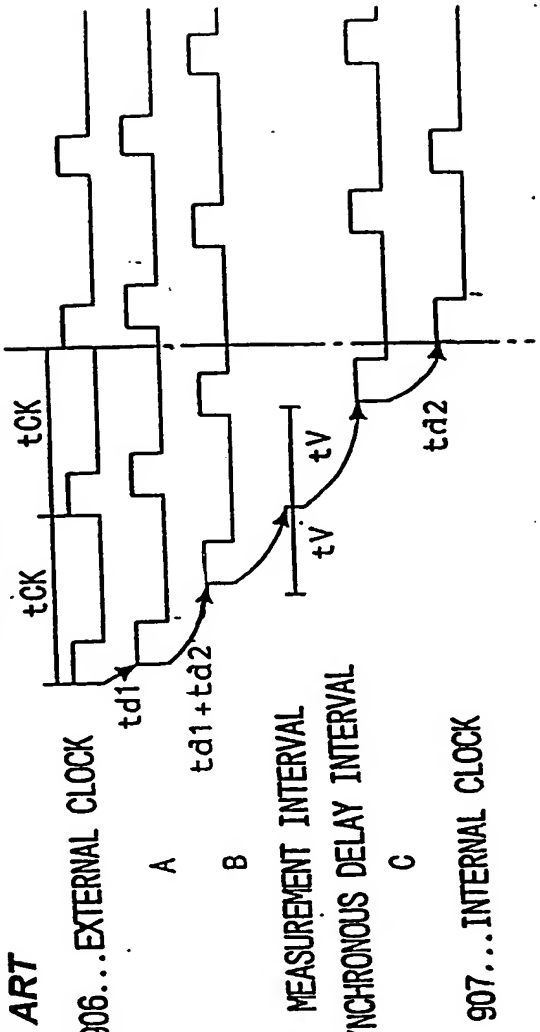


FIG. 23 (b)

RELATED ART



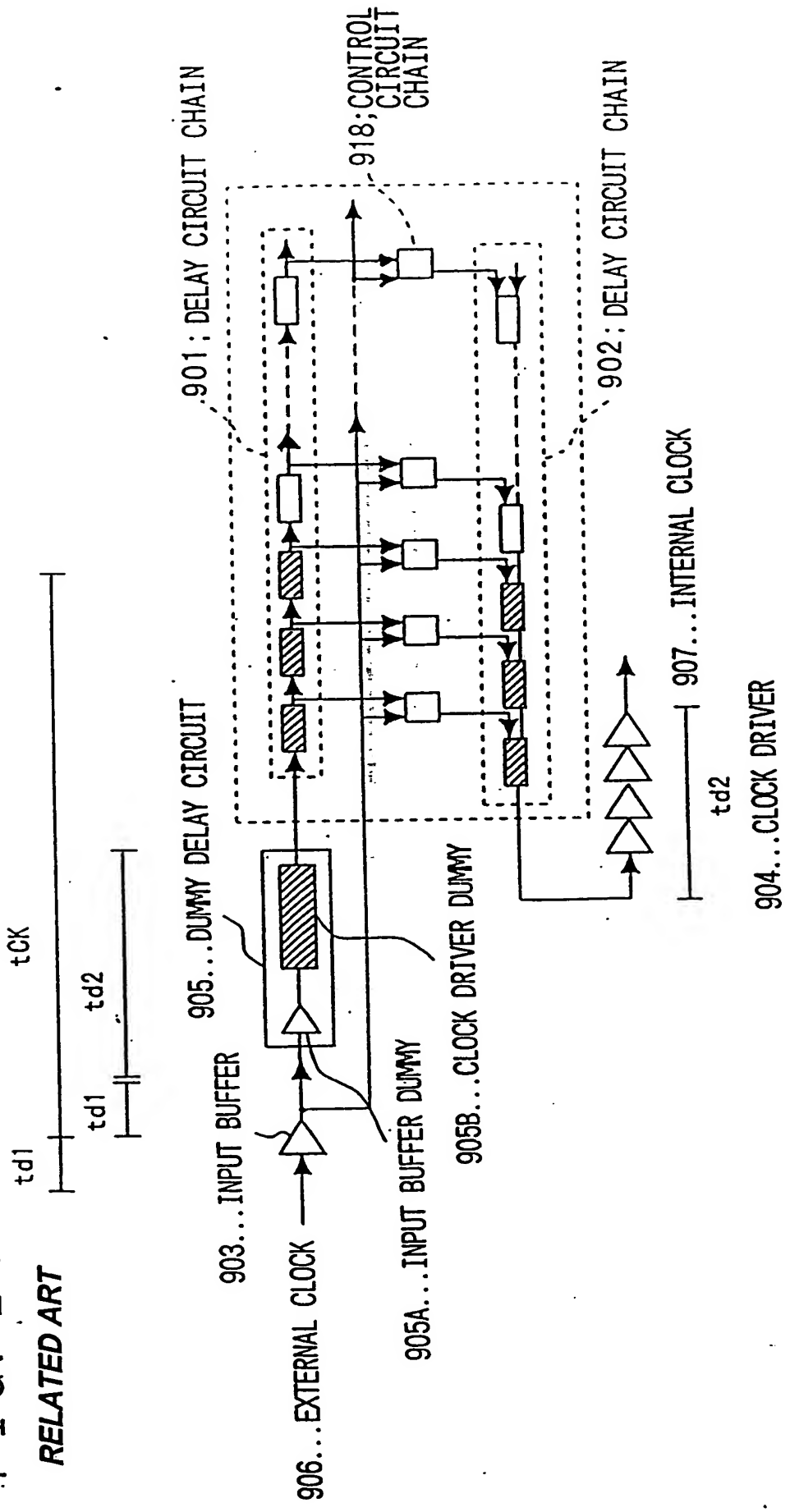


FIG. 24
RELATED ART

FIG. 25
RELATED ART

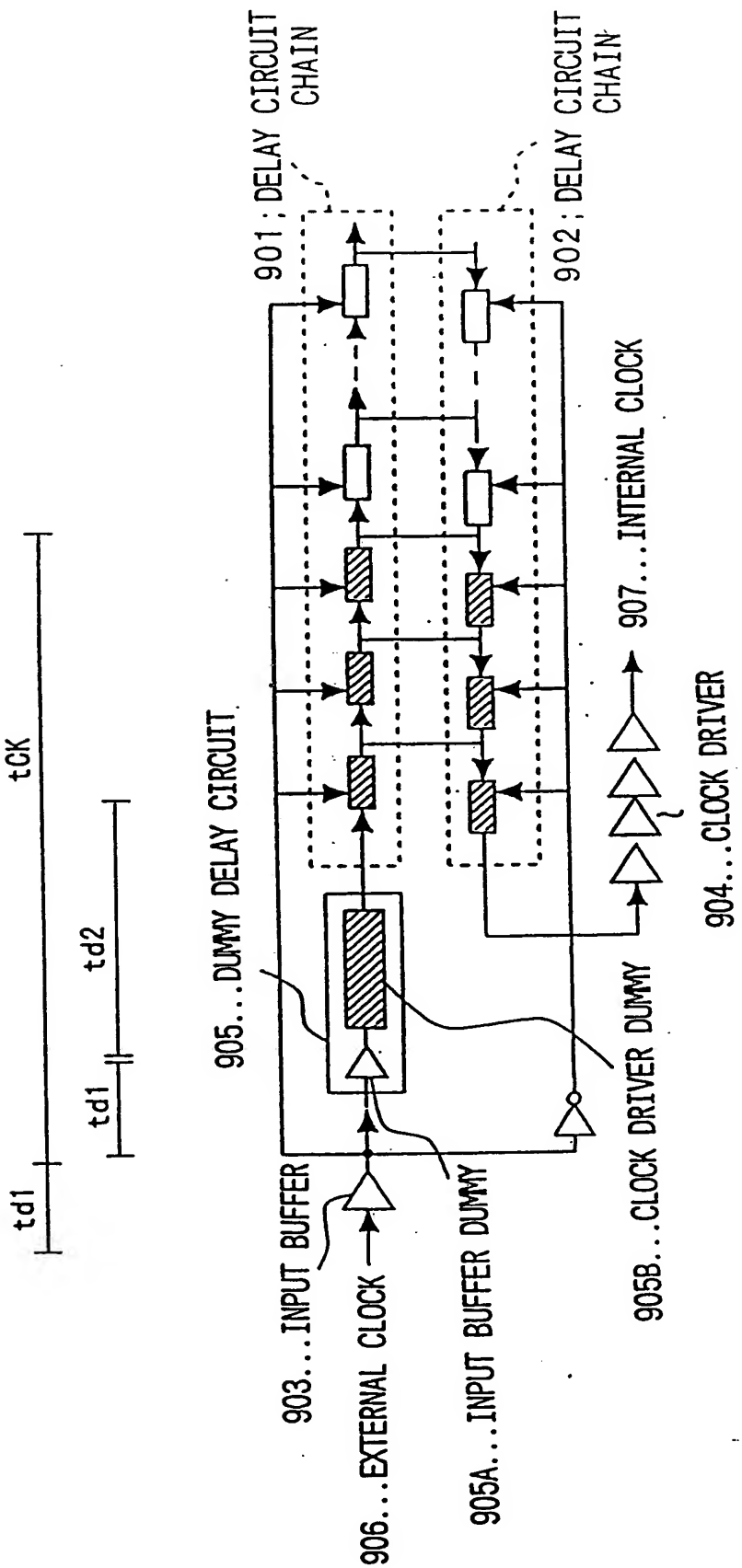
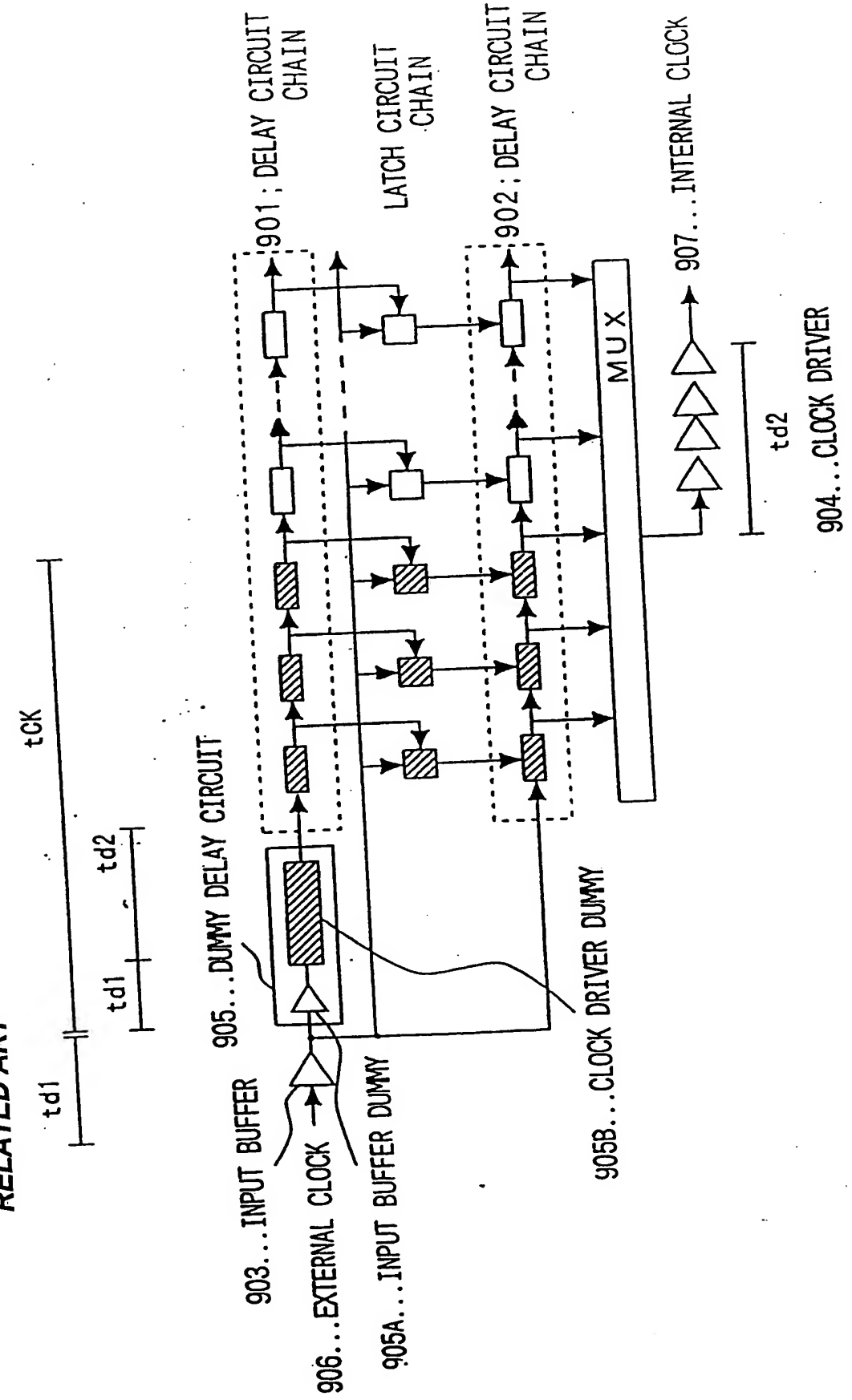


FIG. 26
RELATED ART



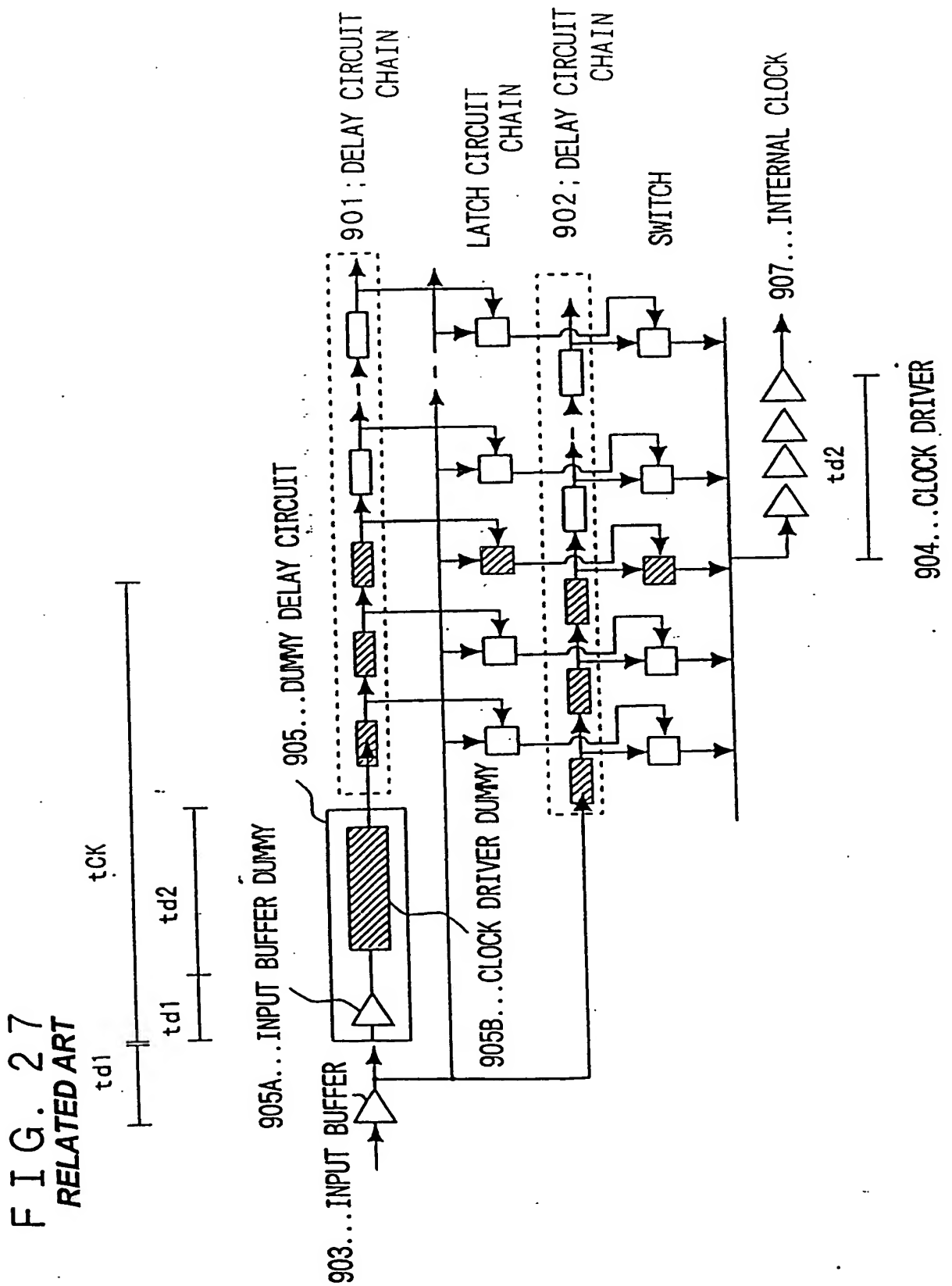


FIG. 27
RELATED ART

FIG. 28(a)

RELATED ART

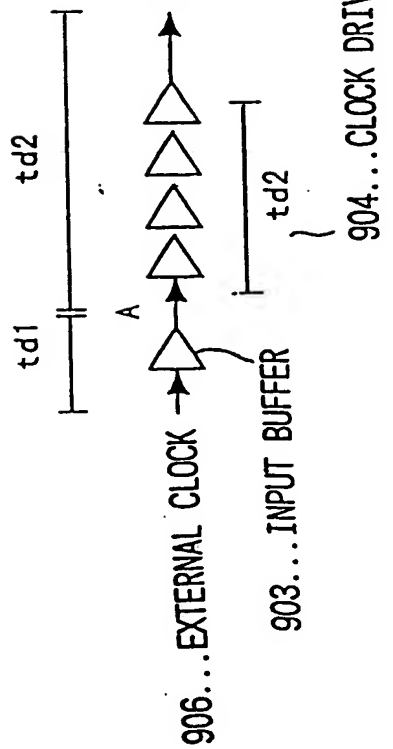


FIG. 28(b)

RELATED ART

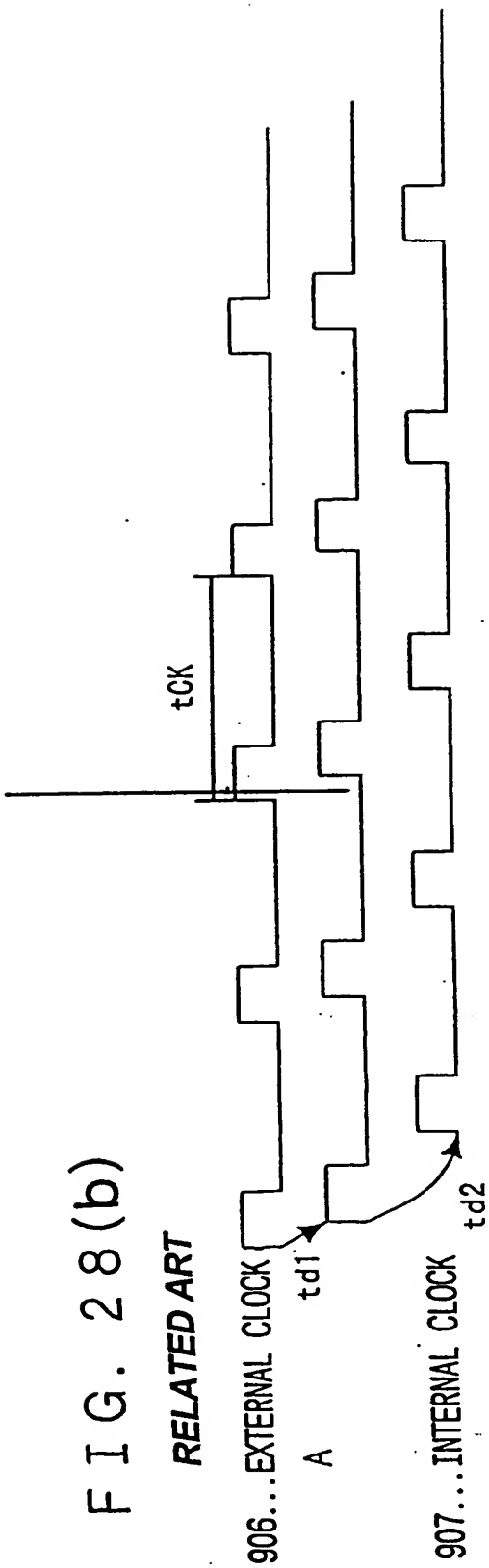


FIG. 29(a)
RELATED ART

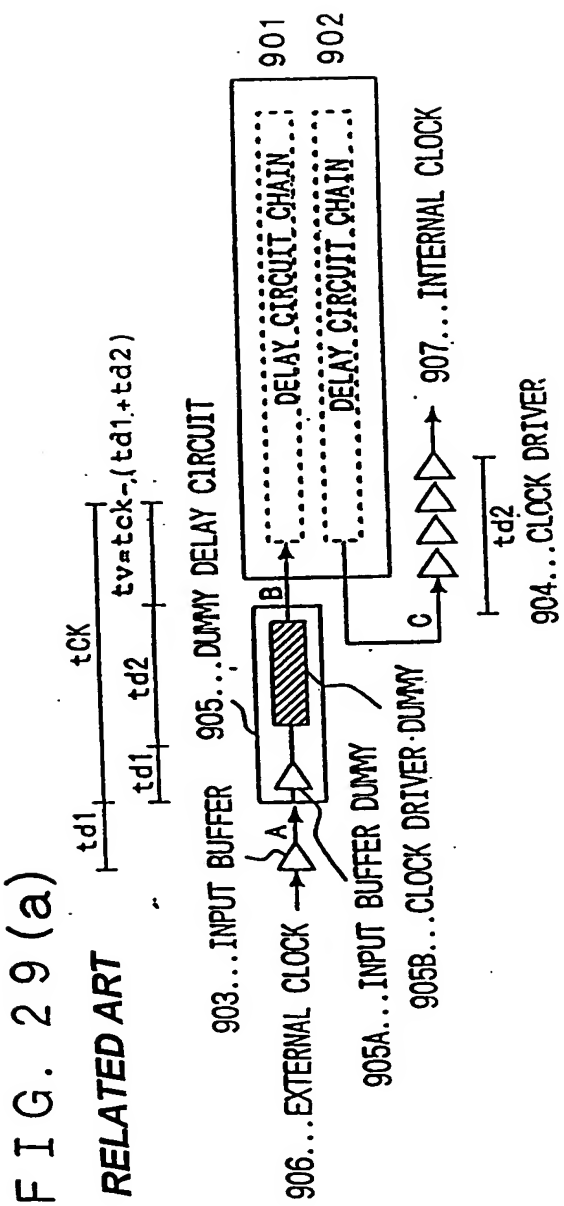


FIG. 29(b)
RELATED ART

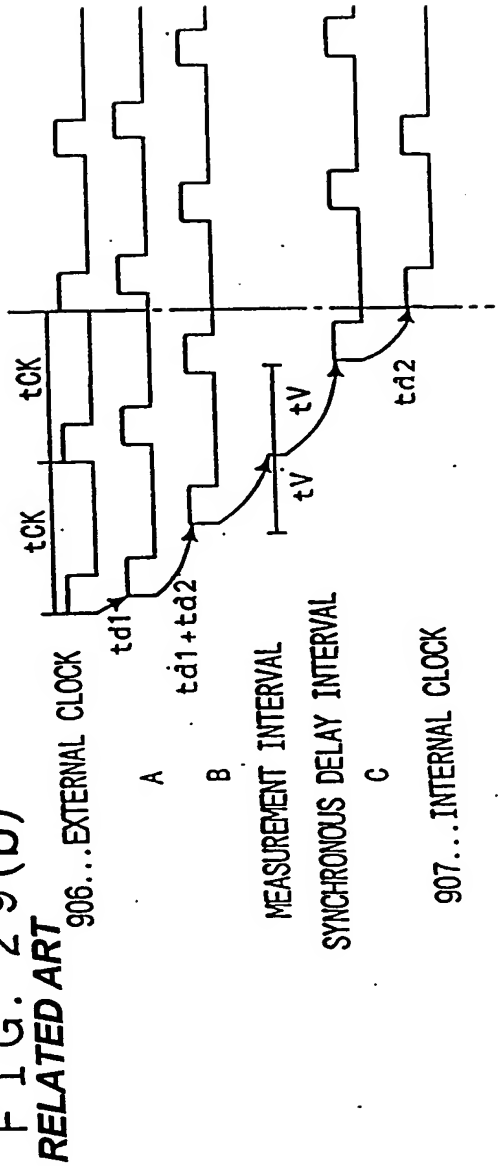


FIG. 30

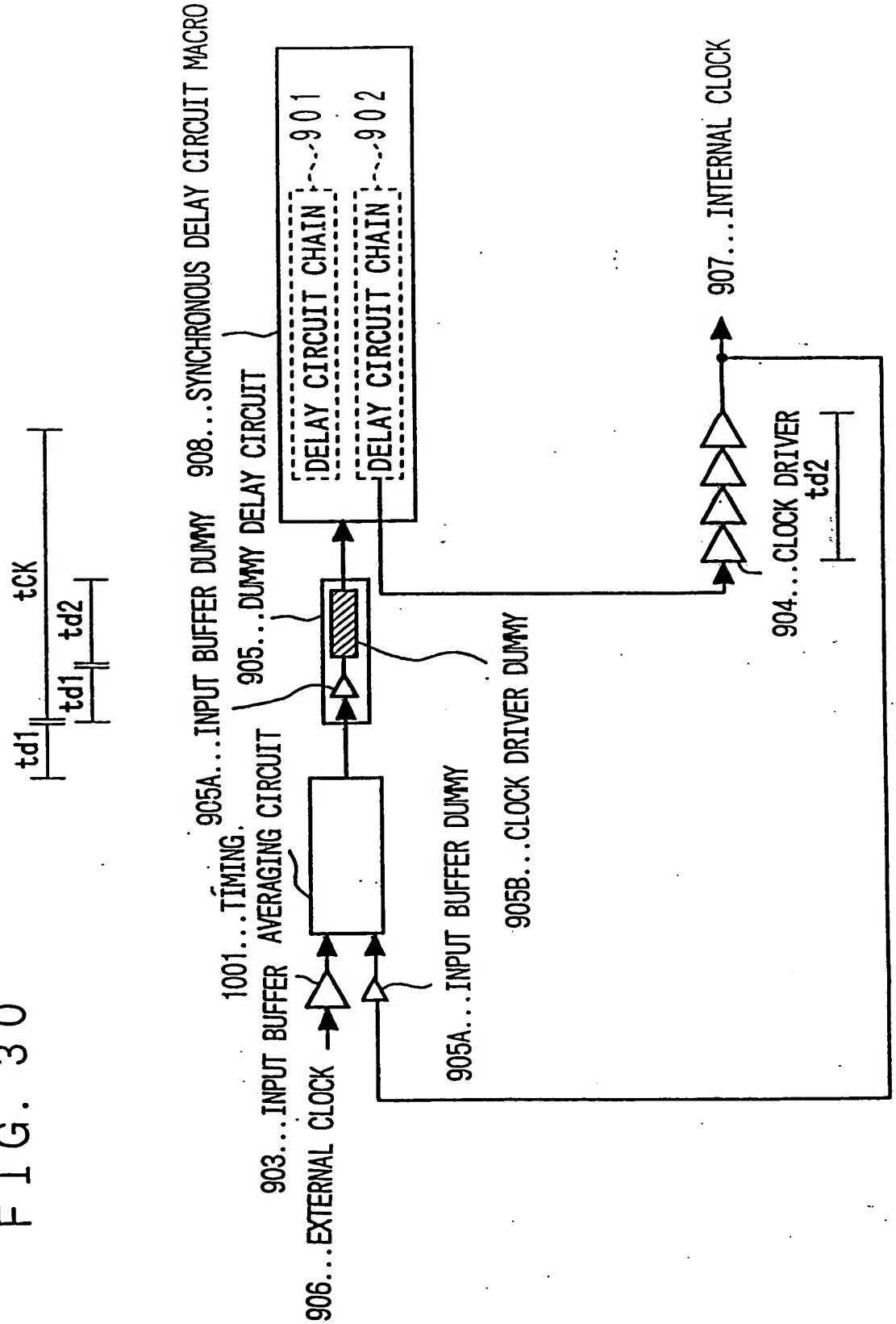

tCK
td1
td2
td1
906...EXTERNAL CLOCK
903...INPUT BUFFER
1001...TIMING AVERAGING CIRCUIT
905A...INPUT BUFFER DUMMY
905...DUMMY DELAY CIRCUIT
908...SYNCHRONOUS DELAY CIRCUIT MACRO
DELAY CIRCUIT CHAIN
901
DELAY CIRCUIT CHAIN
902
905A...INPUT BUFFER DUMMY
905B...CLOCK DRIVER DUMMY
907...INTERNAL CLOCK
904...CLOCK DRIVER
td2

FIG. 31

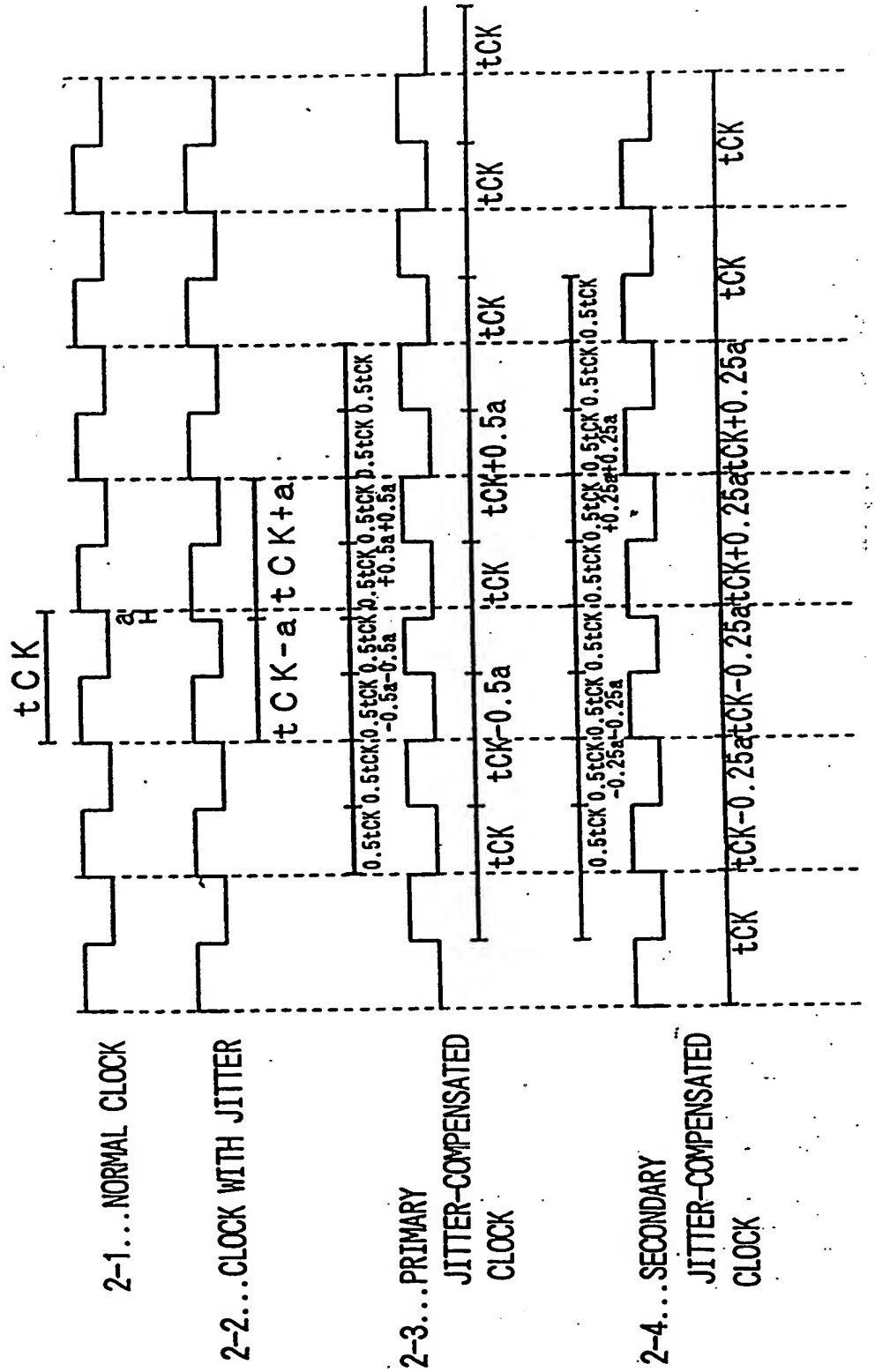

2-1...NORMAL CLOCK
2-2...CLOCK WITH JITTER
2-3...PRIMARY JITTER-COMPENSATED CLOCK
2-4...SECONDARY JITTER-COMPENSATED CLOCK
tCK
a
H
tCK-a
tCK+a
0.5tCK
-0.5a
+0.5a
tCK-0.5a
tCK+0.5a
-0.25a
+0.25a
tCK-0.25a
tCK+0.25a

FIG. 32

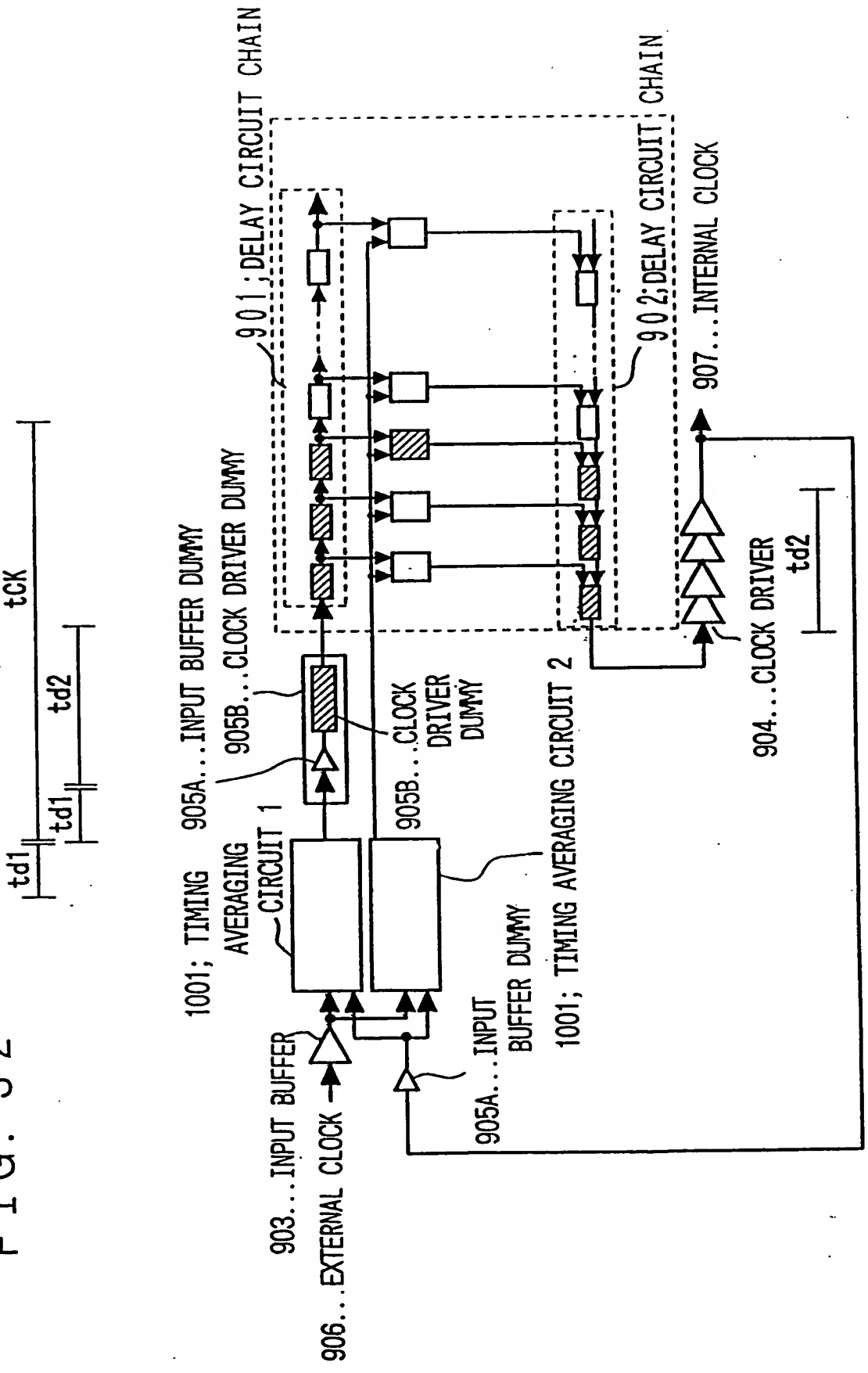

tCK
td2
td1
td1
906...EXTERNAL CLOCK
903...INPUT BUFFER
1001; TIMING AVERAGING CIRCUIT 1
905A...INPUT BUFFER DUMMY
905B...CLOCK DRIVER DUMMY
901;DELAY CIRCUIT CHAIN
905A...INPUT BUFFER DUMMY
905B...CLOCK DRIVER DUMMY
1001; TIMING AVERAGING CIRCUIT 2
902;DELAY CIRCUIT CHAIN
907...INTERNAL CLOCK
904...CLOCK DRIVER
td2

FIG. 33

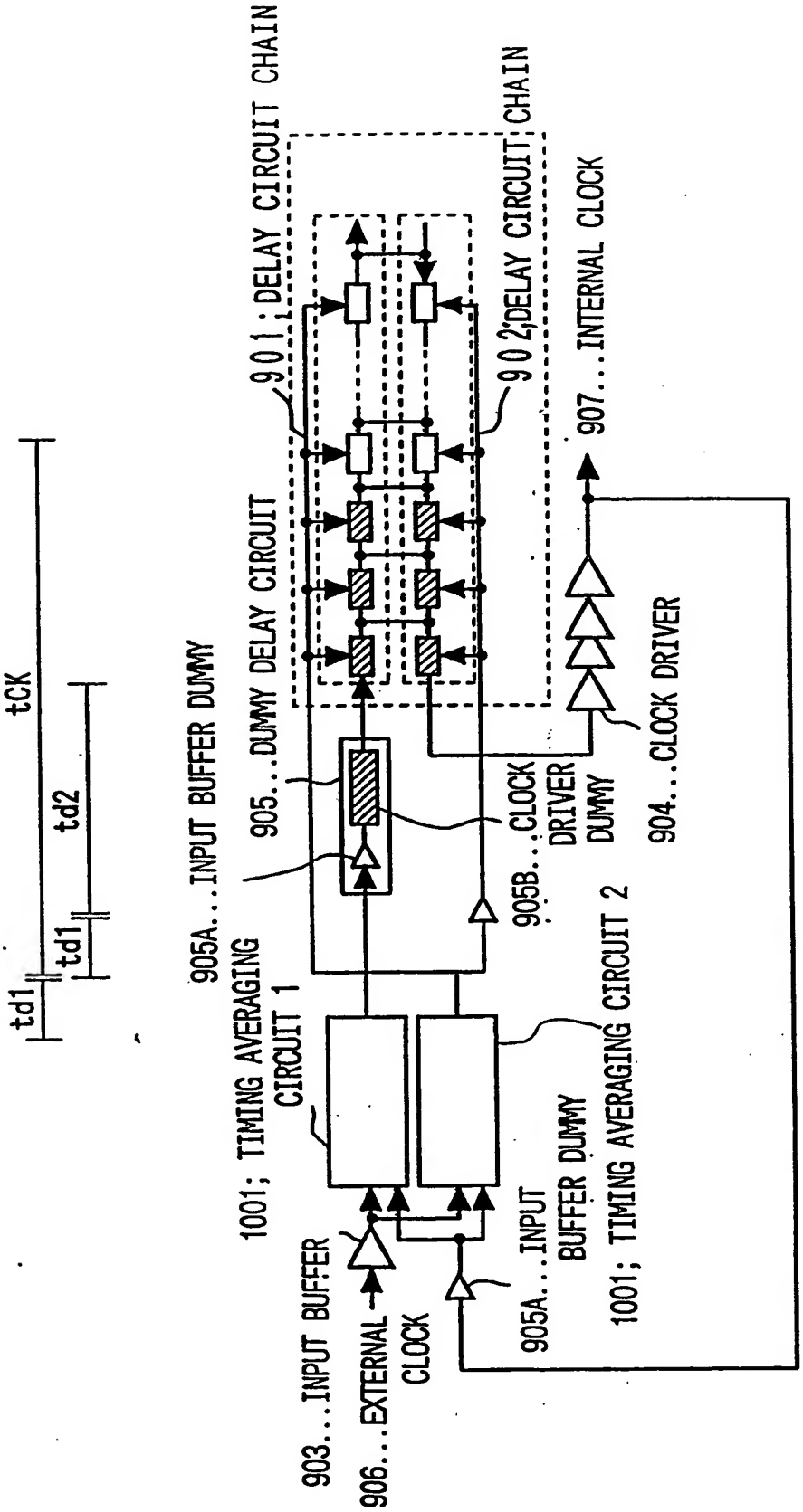

tCK
td2
td1
td1
901; DELAY CIRCUIT CHAIN
902;DELAY CIRCUIT CHAIN
907...INTERNAL CLOCK
905A...INPUT BUFFER DUMMY
905...DUMMY DELAY CIRCUIT
905B...CLOCK DRIVER DUMMY
904...CLOCK DRIVER
1001; TIMING AVERAGING CIRCUIT 1
1001; TIMING AVERAGING CIRCUIT 2
903...INPUT BUFFER
906...EXTERNAL CLOCK
905A...INPUT BUFFER DUMMY

FIG. 34

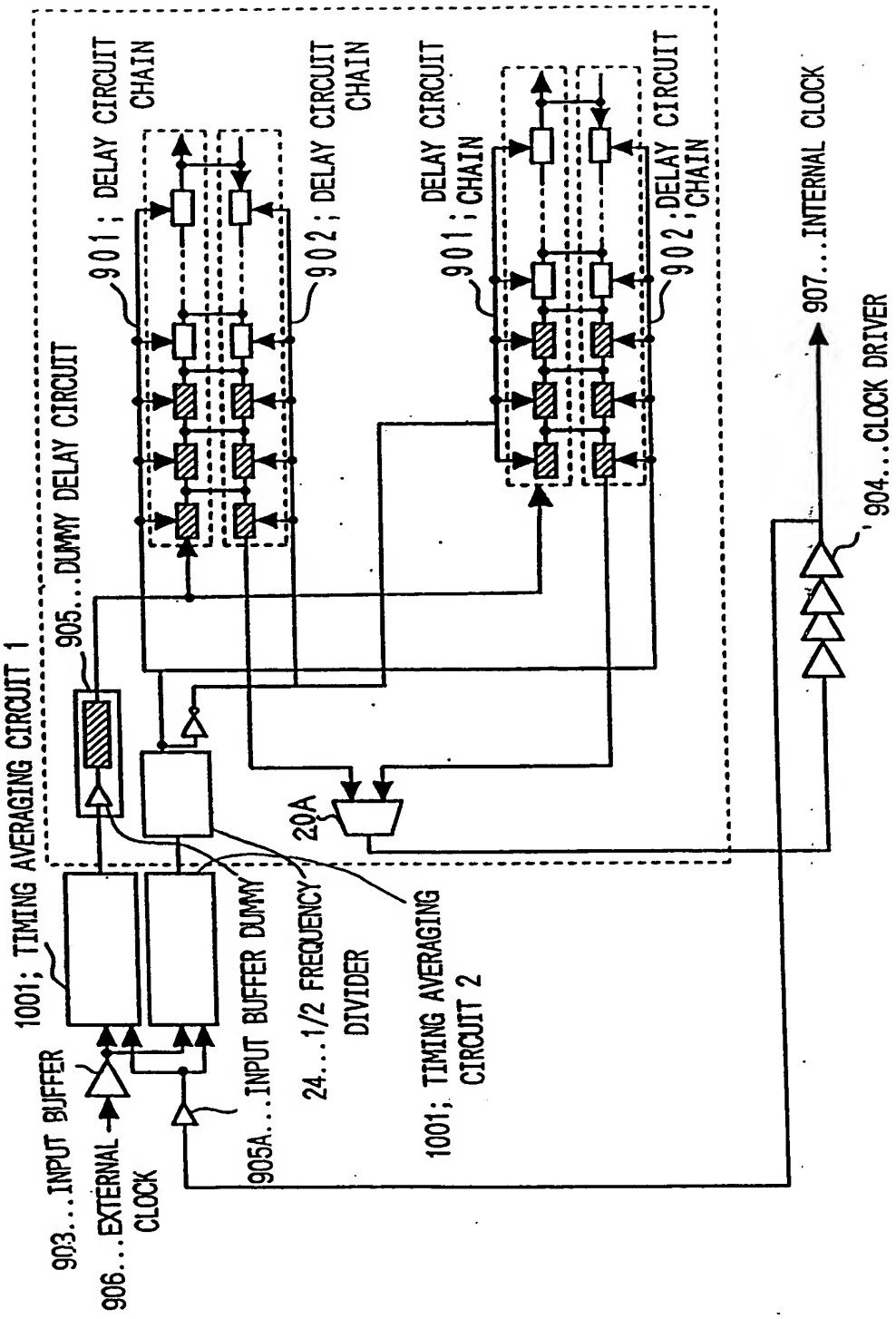

1001; TIMING AVERAGING CIRCUIT 1
905...DUMMY DELAY CIRCUIT
901; DELAY CIRCUIT CHAIN
902; DELAY CIRCUIT CHAIN
901; DELAY CIRCUIT CHAIN
902; DELAY CIRCUIT CHAIN
907...INTERNAL CLOCK
904...CLOCK DRIVER
20A
1001; TIMING AVERAGING CIRCUIT 2
24...1/2 FREQUENCY DIVIDER
905A...INPUT BUFFER DUMMY
903...INPUT BUFFER
906...EXTERNAL CLOCK

FIG. 35

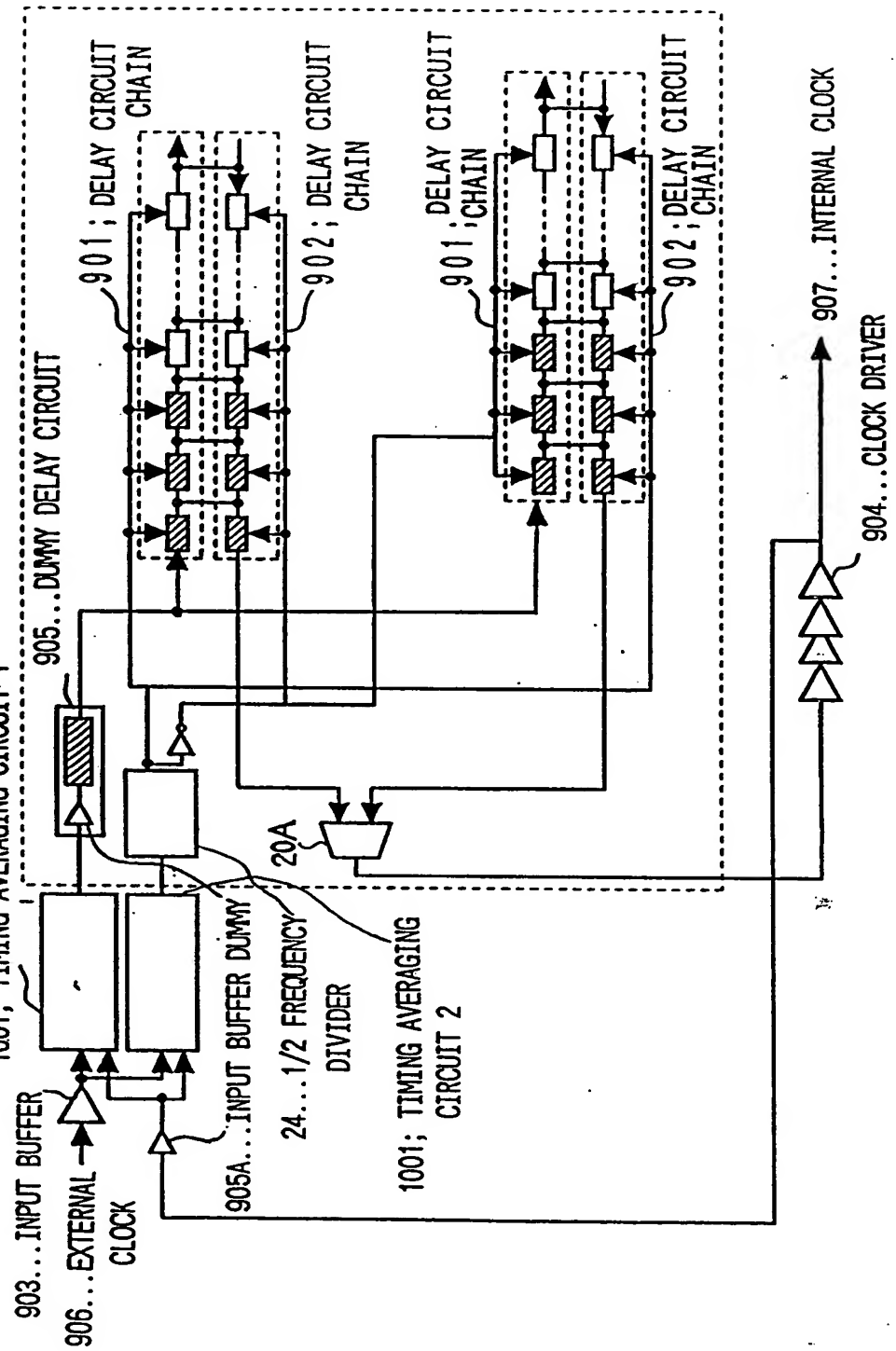

1001; TIMING AVERAGING CIRCUIT 1
905...DUMMY DELAY CIRCUIT
901; DELAY CIRCUIT CHAIN
902; DELAY CIRCUIT CHAIN
901; DELAY CIRCUIT CHAIN
902; DELAY CIRCUIT CHAIN
907...INTERNAL CLOCK
904...CLOCK DRIVER
20A
903...INPUT BUFFER
906...EXTERNAL CLOCK
905A...INPUT BUFFER DUMMY
24...1/2 FREQUENCY DIVIDER
1001; TIMING AVERAGING CIRCUIT 2

FIG. 36

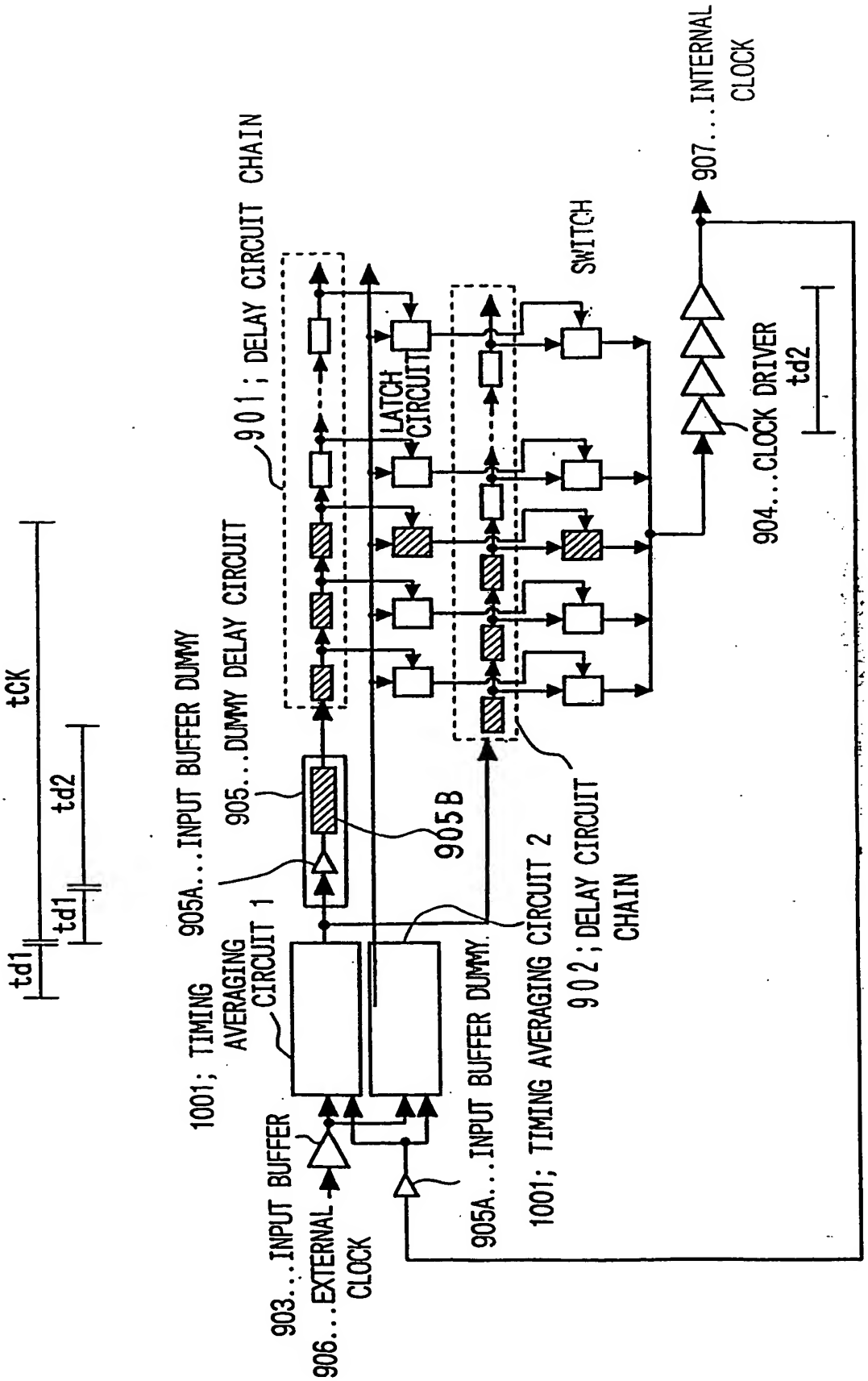

tCK
td2
td1
td1
901; DELAY CIRCUIT CHAIN
905...DUMMY DELAY CIRCUIT
905A...INPUT BUFFER DUMMY
905B
LATCH CIRCUIT
SWITCH
907...INTERNAL CLOCK
904...CLOCK DRIVER
td2
1001; TIMING AVERAGING CIRCUIT 1
903...INPUT BUFFER
906...EXTERNAL CLOCK
905A...INPUT BUFFER DUMMY
1001; TIMING AVERAGING CIRCUIT 2
902; DELAY CIRCUIT CHAIN

FIG. 37(a)

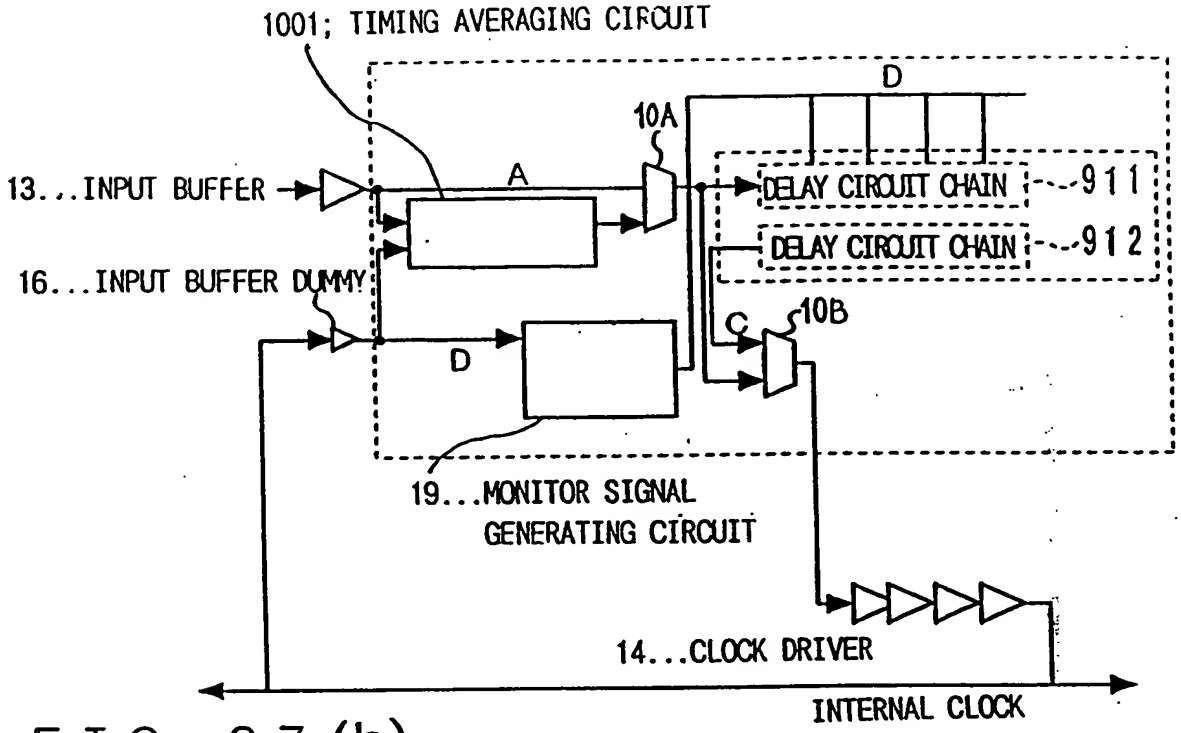


FIG. 37(b)

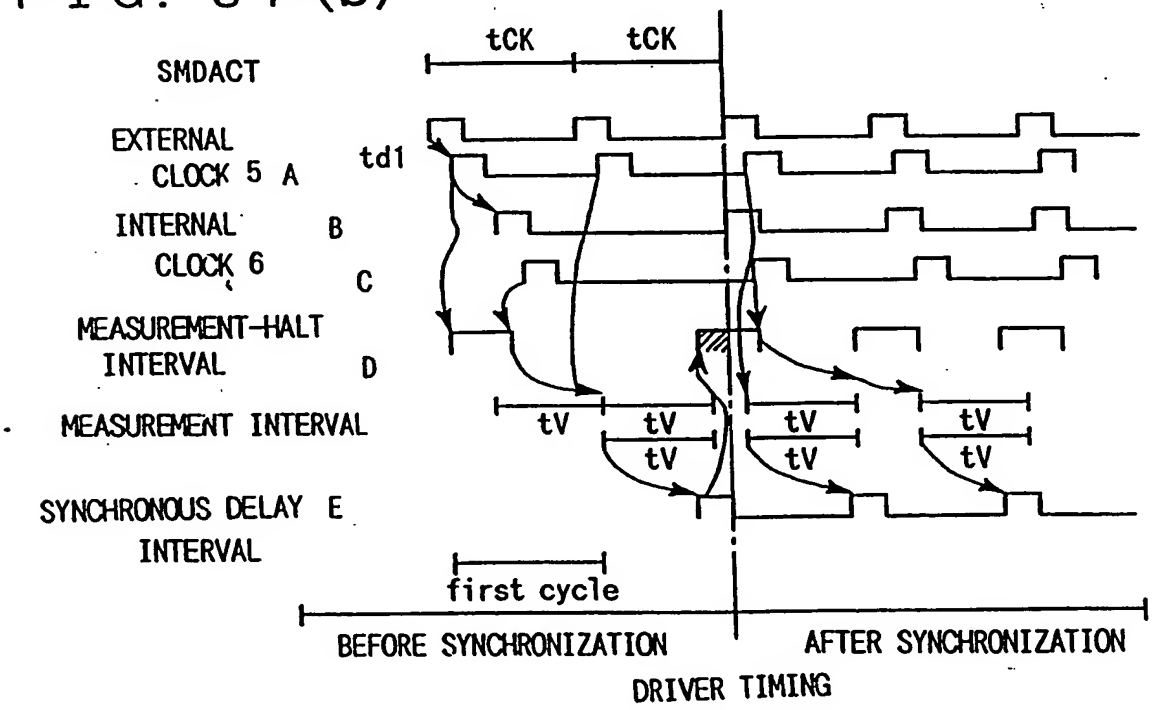


FIG. 38

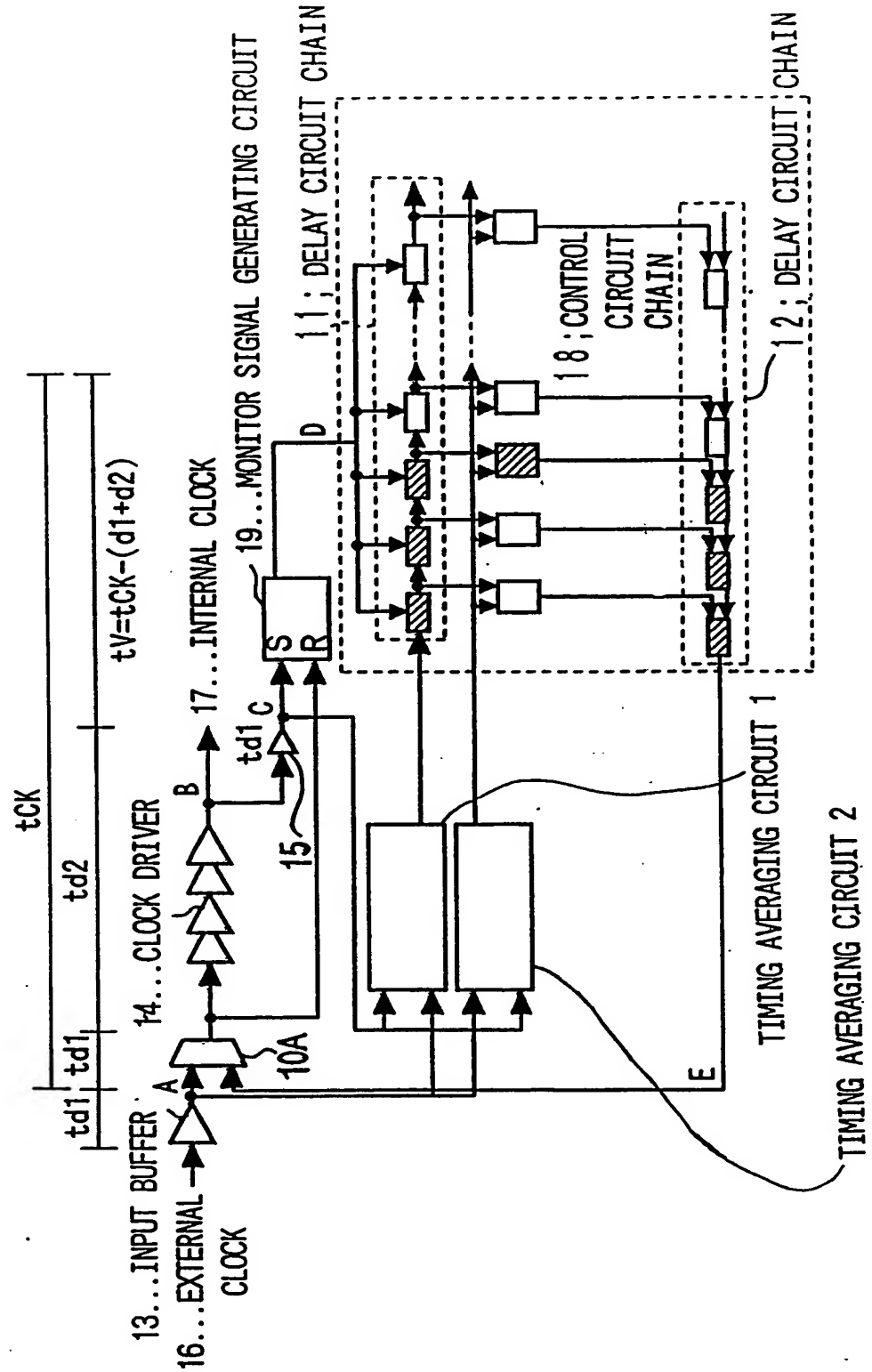

tCK
td2
tV=tCK-(d1+d2)
td1
td1
13...INPUT BUFFER
16...EXTERNAL CLOCK
14...CLOCK DRIVER
10A
A
B
15
td1
C
17...INTERNAL CLOCK
19...MONITOR SIGNAL GENERATING CIRCUIT
S
R
D
11; DELAY CIRCUIT CHAIN
18; CONTROL CIRCUIT CHAIN
12; DELAY CIRCUIT CHAIN
E
TIMING AVERAGING CIRCUIT 1
TIMING AVERAGING CIRCUIT 2

FIG. 39

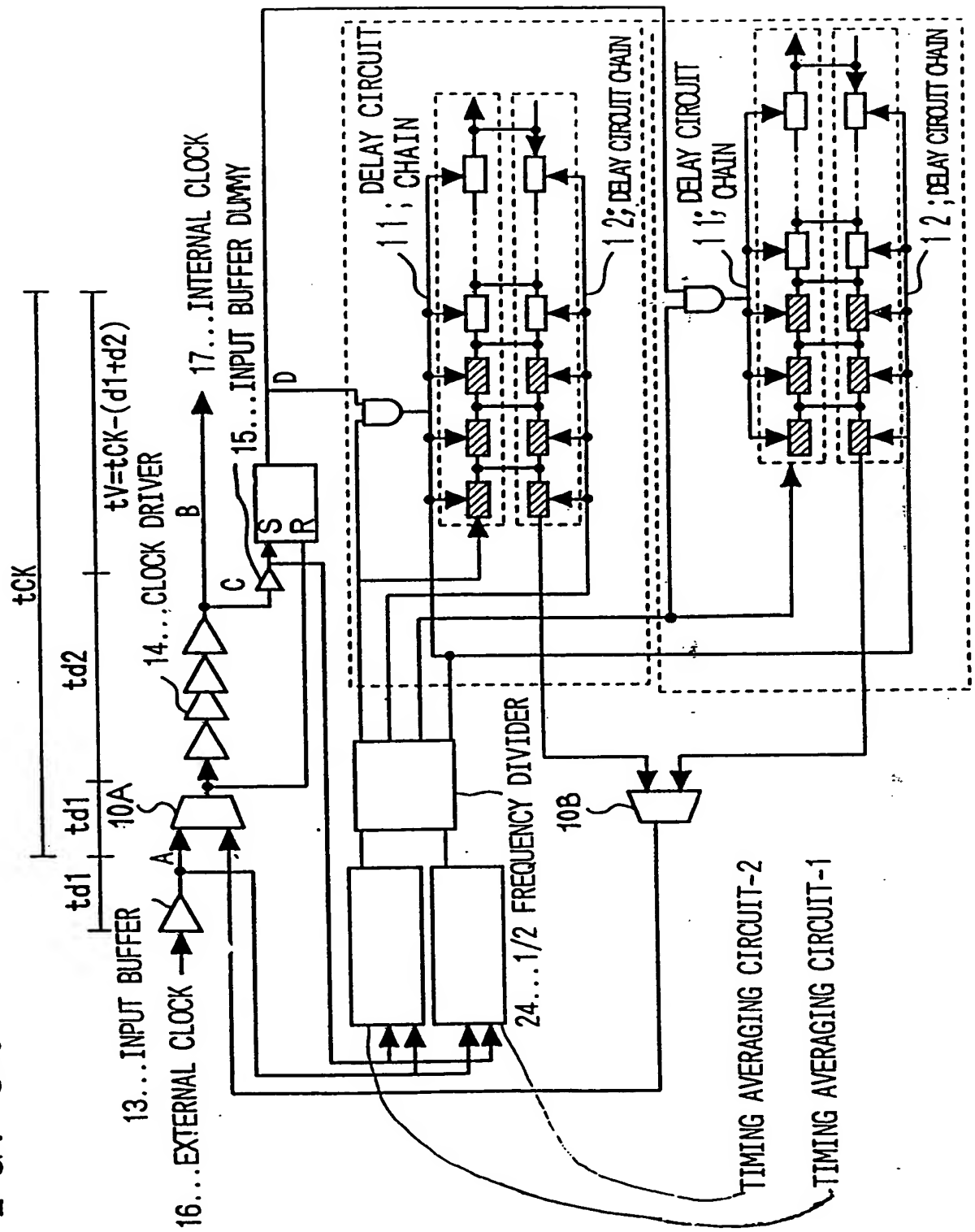

tCK
td2
tV=tCK-(d1+d2)
td1
td1
10A
A
B
C
D
S
R
13...INPUT BUFFER
16...EXTERNAL CLOCK
14...CLOCK DRIVER
15...INPUT BUFFER DUMMY
17...INTERNAL CLOCK
DELAY CIRCUIT
11; CHAIN
12; DELAY CIRCUIT CHAIN
DELAY CIRCUIT
11; CHAIN
12; DELAY CIRCUIT CHAIN
24...1/2 FREQUENCY DIVIDER
10B
TIMING AVERAGING CIRCUIT-2
TIMING AVERAGING CIRCUIT-1

FIG. 40

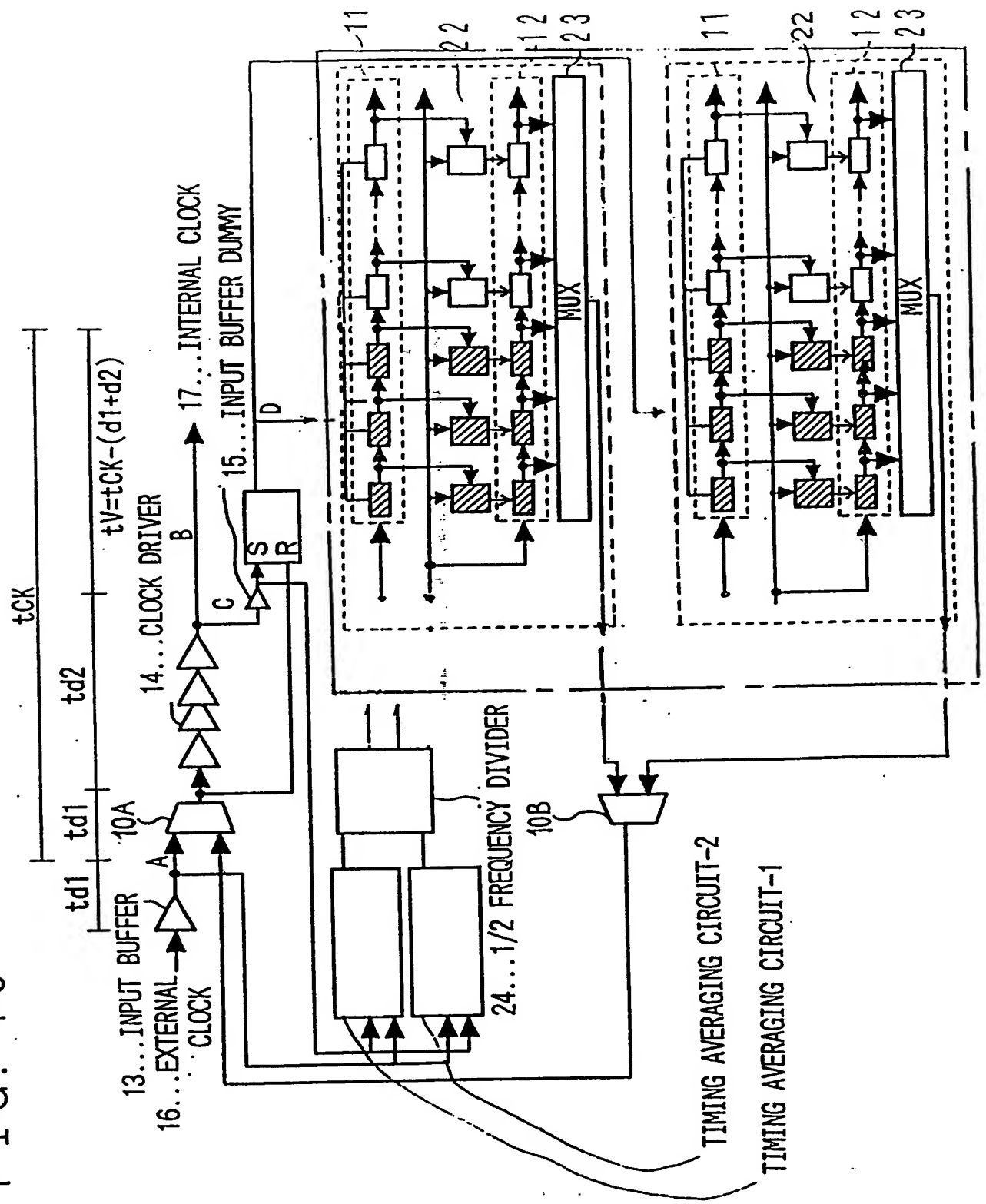

tCK
td1
td2
td1
tV=tCK-(d1+d2)
13...INPUT BUFFER
16...EXTERNAL CLOCK
A
10A
14...CLOCK DRIVER
B
C
17...INTERNAL CLOCK
15...INPUT BUFFER DUMMY
D
S
R
24...1/2 FREQUENCY DIVIDER
10B
MUX
MUX
11
22
12
23
11
22
12
23
TIMING AVERAGING CIRCUIT-2
TIMING AVERAGING CIRCUIT-1

FIG. 41

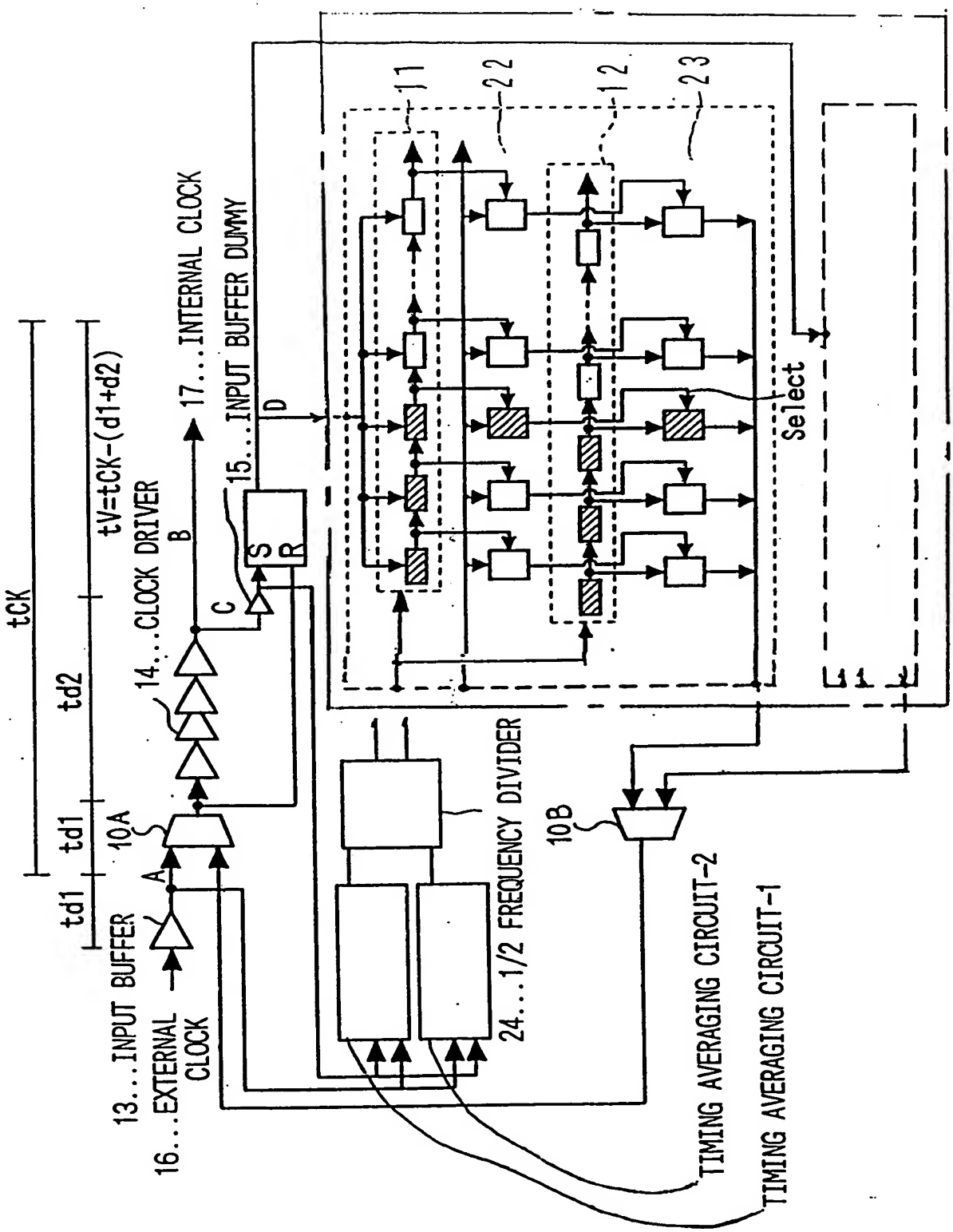

tCK
td2
tV=tCK-(d1+d2)
td1
td1
13...INPUT BUFFER
16...EXTERNAL CLOCK
A
10A
14...CLOCK DRIVER
B
C
17...INTERNAL CLOCK
15...INPUT BUFFER DUMMY
D
S
R
11
22
12
23
Select
24...1/2 FREQUENCY DIVIDER
10B
TIMING AVERAGING CIRCUIT-2
TIMING AVERAGING CIRCUIT-1

FIG. 42

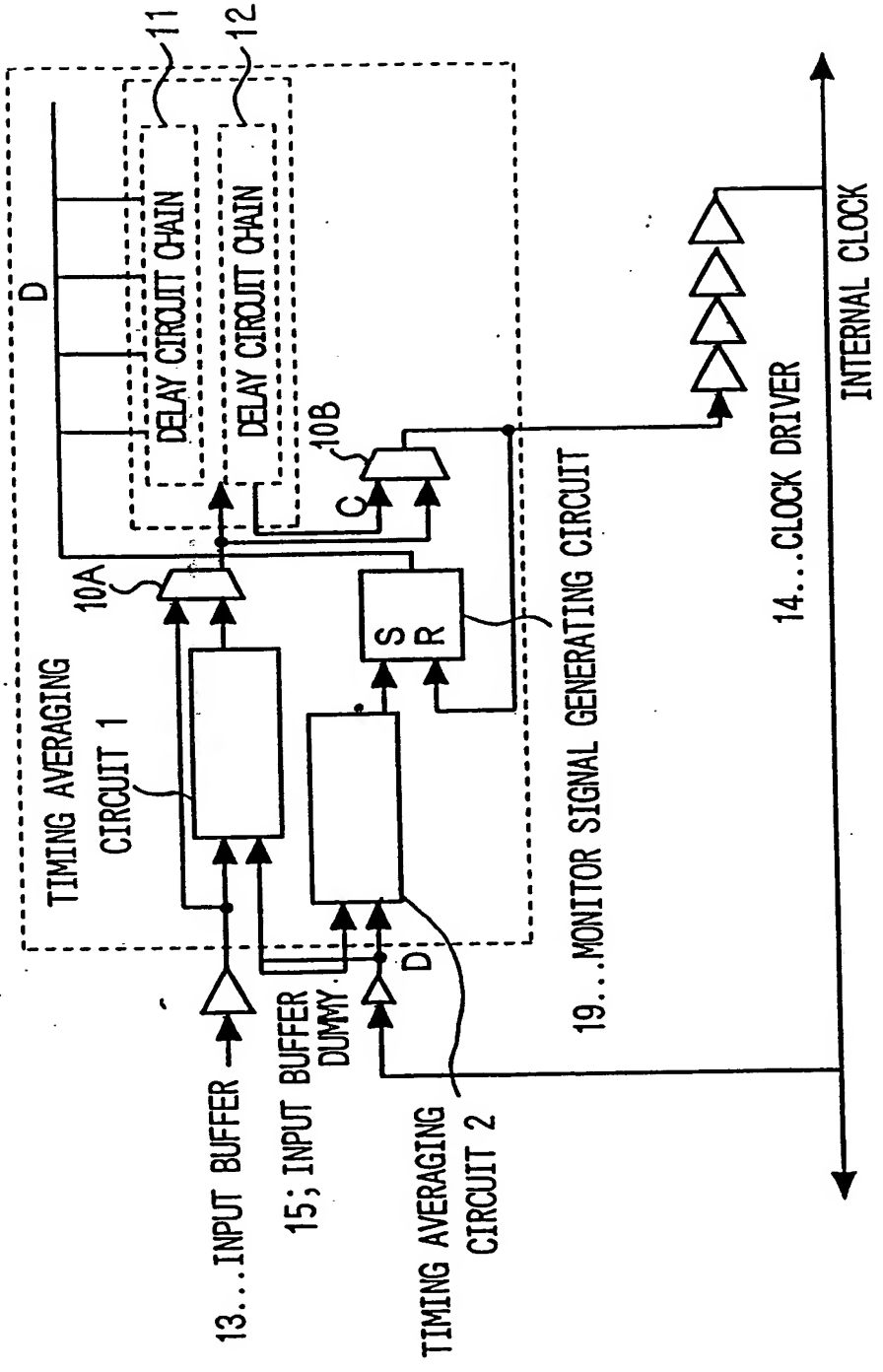
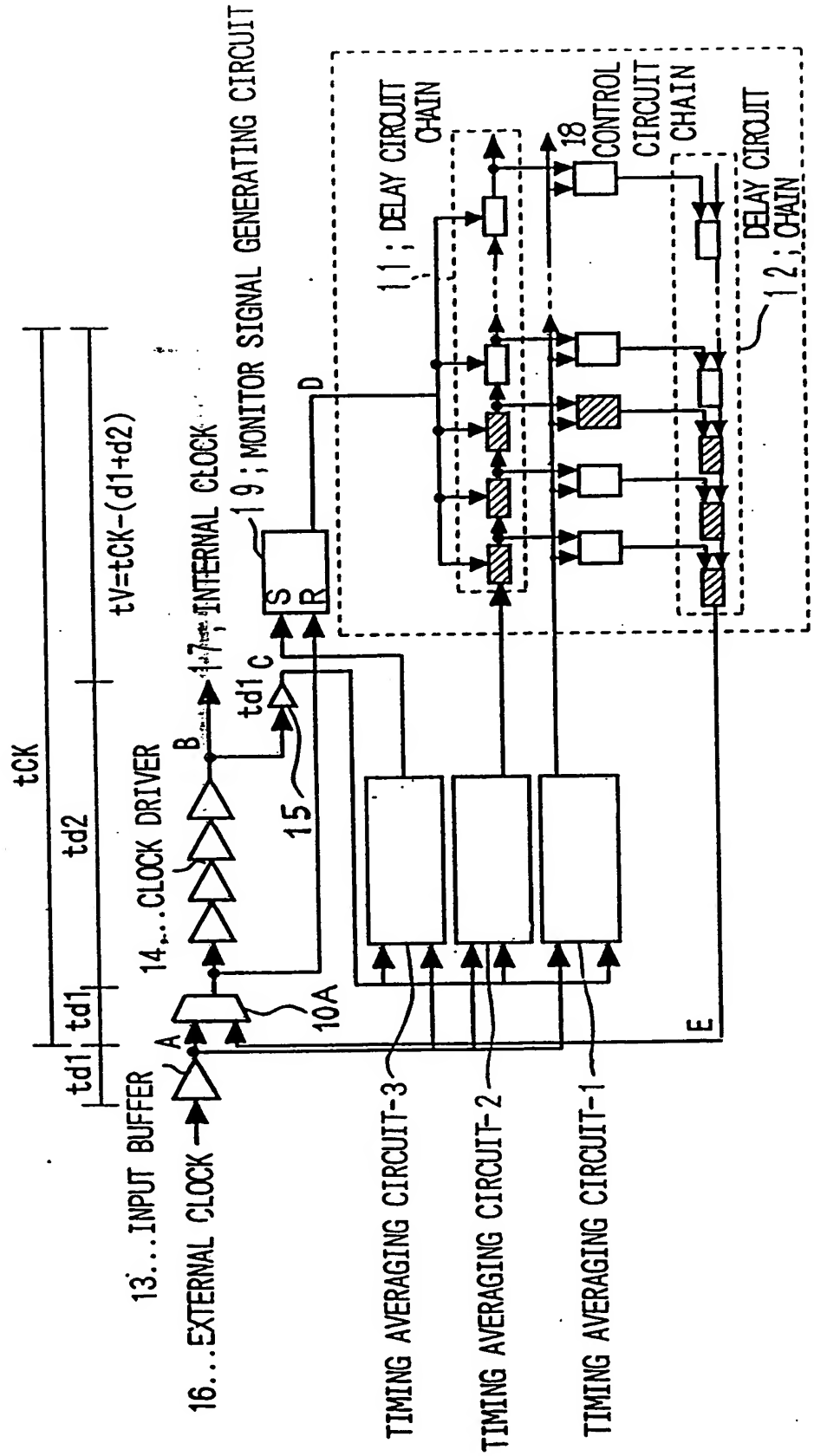

11
12
D
DELAY CIRCUIT CHAIN
DELAY CIRCUIT CHAIN
10B
C
10A
S
R
TIMING AVERAGING CIRCUIT 1
D
19...MONITOR SIGNAL GENERATING CIRCUIT
14...CLOCK DRIVER
INTERNAL CLOCK
13...INPUT BUFFER
15; INPUT BUFFER DUMMY
TIMING AVERAGING CIRCUIT 2

FIG. 43


tCK
td2
tV=tCK-(d1+d2)
td1
td1
13...INPUT BUFFER
16...EXTERNAL CLOCK
A
14...CLOCK DRIVER
B
10A
17; INTERNAL CLOCK
td1
C
15
19; MONITOR SIGNAL GENERATING CIRCUIT
D
S
R
11; DELAY CIRCUIT CHAIN
18
CONTROL CIRCUIT
DELAY CIRCUIT CHAIN
12; CHAIN
E
TIMING AVERAGING CIRCUIT-3
TIMING AVERAGING CIRCUIT-2
TIMING AVERAGING CIRCUIT-1

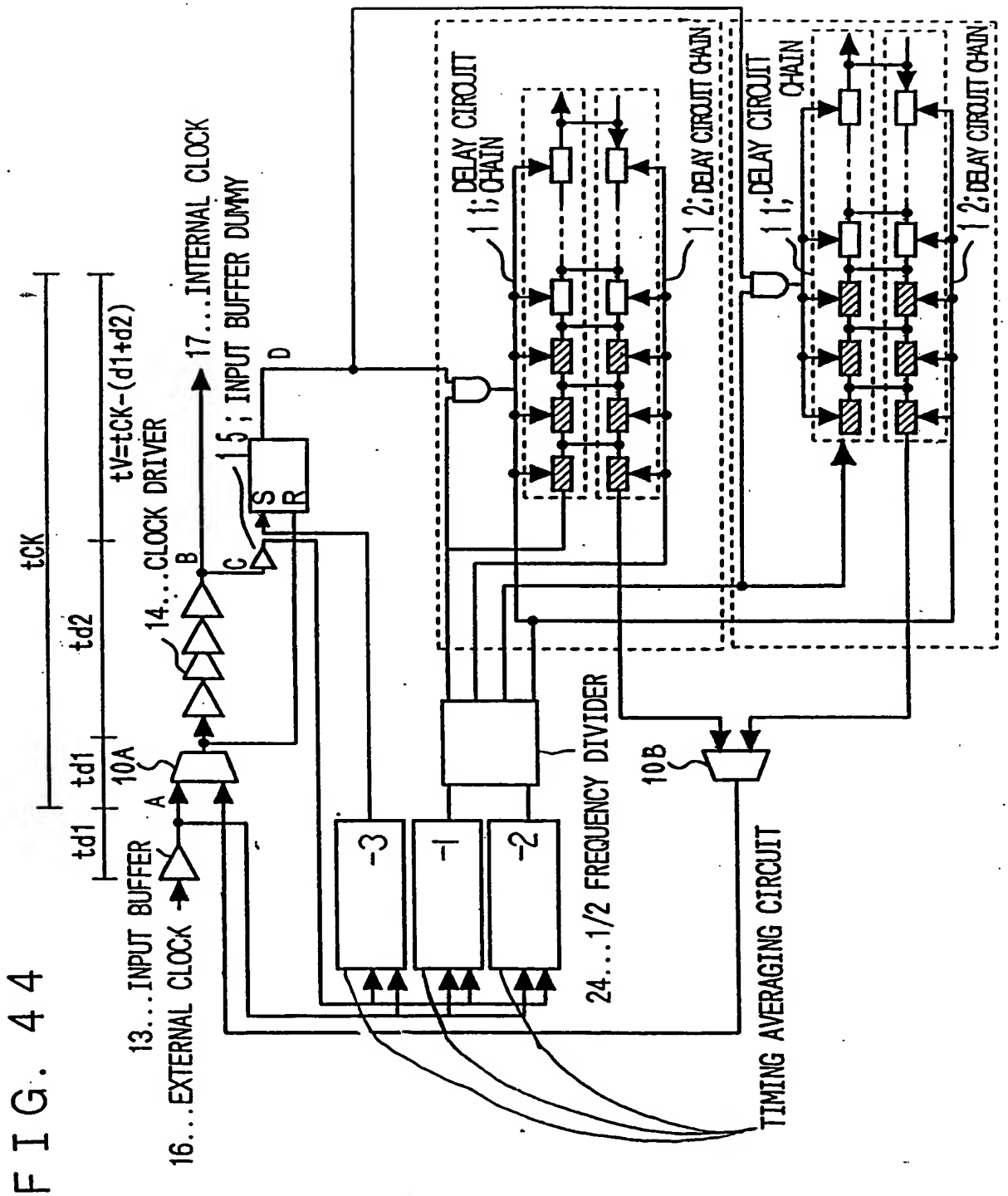

tCK
tV=tCK-(d1+d2)
td2
td1
td1
10A
A
B
C
D
S
R
13...INPUT BUFFER
16...EXTERNAL CLOCK
14...CLOCK DRIVER
15; INPUT BUFFER DUMMY
17...INTERNAL CLOCK
11; DELAY CIRCUIT CHAIN
12; DELAY CIRCUIT CHAIN
11; DELAY CIRCUIT CHAIN
12; DELAY CIRCUIT CHAIN
-3
-1
-2
24...1/2 FREQUENCY DIVIDER
10B
TIMING AVERAGING CIRCUIT

FIG. 44

FIG. 45

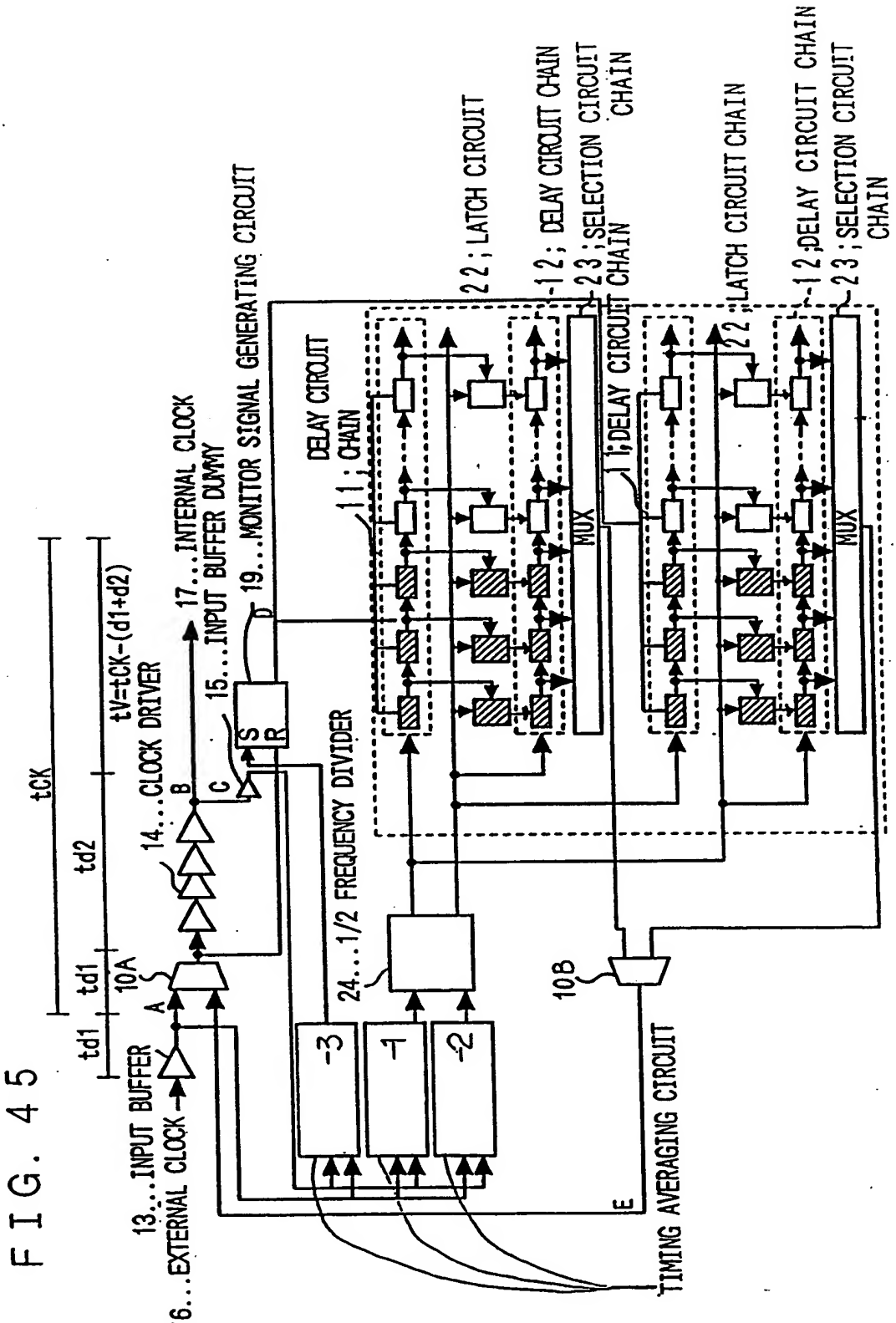

tCK
td1
td2
tV=tCK-(d1+d2)
td1
13...INPUT BUFFER
16...EXTERNAL CLOCK
10A
A
14...CLOCK DRIVER
B
C
15...INPUT BUFFER DUMMY
17...INTERNAL CLOCK
19...MONITOR SIGNAL GENERATING CIRCUIT
S
R
D
11; DELAY CIRCUIT CHAIN
24...1/2 FREQUENCY DIVIDER
-3
-1
-2
E
TIMING AVERAGING CIRCUIT
10B
22; LATCH CIRCUIT
12; DELAY CIRCUIT CHAIN
23; SELECTION CIRCUIT CHAIN
MUX
22; LATCH CIRCUIT CHAIN
12; DELAY CIRCUIT CHAIN
23; SELECTION CIRCUIT CHAIN
MUX

FIG. 46

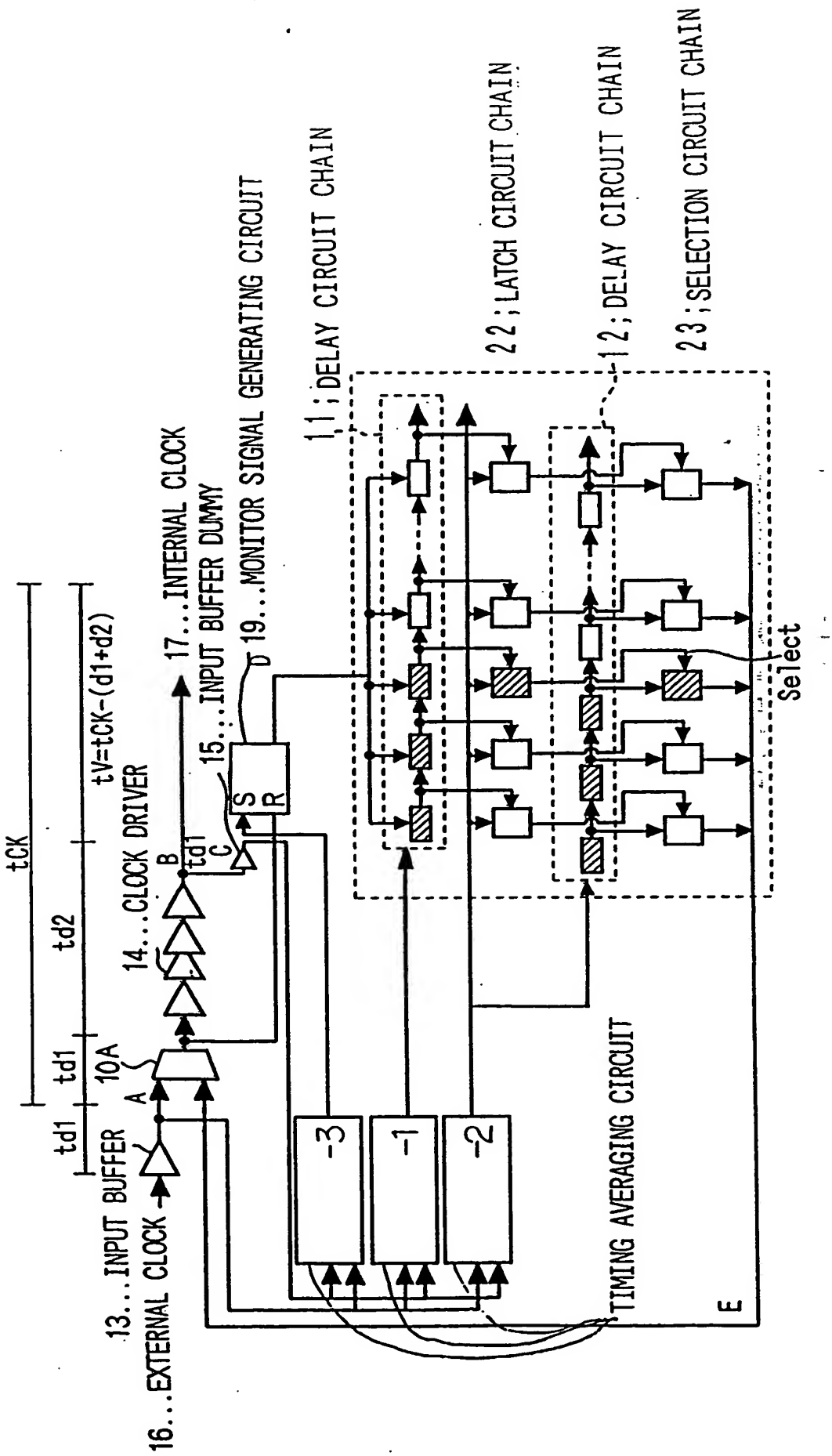

16...EXTERNAL CLOCK
13...INPUT BUFFER
10A
14...CLOCK DRIVER
17...INTERNAL CLOCK
15...INPUT BUFFER DUMMY
19...MONITOR SIGNAL GENERATING CIRCUIT
11;DELAY CIRCUIT CHAIN
22;LATCH CIRCUIT CHAIN
12;DELAY CIRCUIT CHAIN
23;SELECTION CIRCUIT CHAIN
TIMING AVERAGING CIRCUIT
Select
tCK
td1
td2
tV=tCK-(d1+d2)
A
B
C
D
E
S
R
-3
-1
-2

FIG. 47

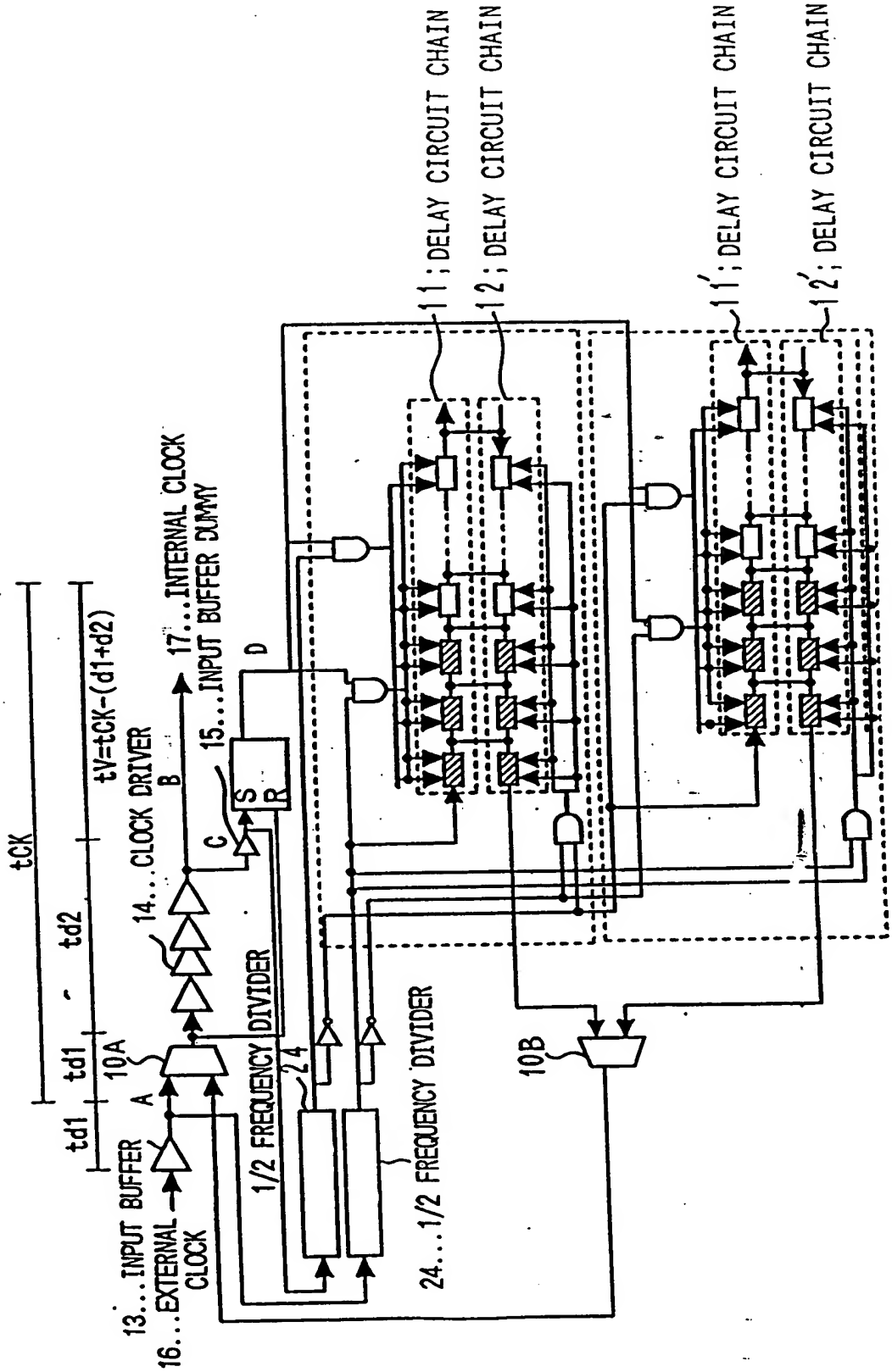

tCK
td1
td2
tV=tCK-(d1+d2)
td1
10A
A
B
C
D
S
R
14...CLOCK DRIVER
15...INPUT BUFFER DUMMY
17...INTERNAL CLOCK
13...INPUT BUFFER
16...EXTERNAL CLOCK
1/2 FREQUENCY DIVIDER
24
24...1/2 FREQUENCY DIVIDER
10B
11; DELAY CIRCUIT CHAIN
12; DELAY CIRCUIT CHAIN
11'; DELAY CIRCUIT CHAIN
12'; DELAY CIRCUIT CHAIN

FIG. 48

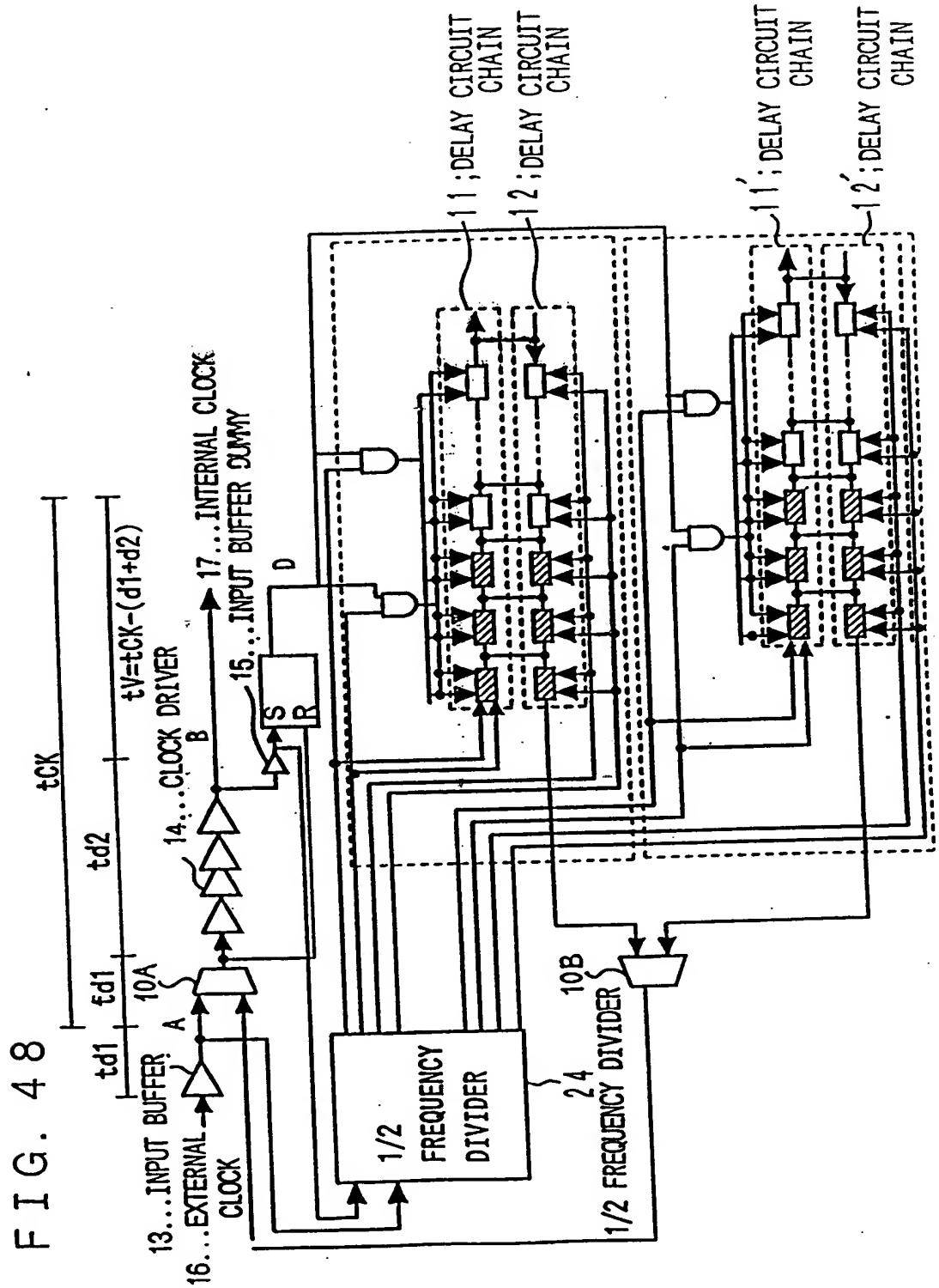

tCK
td2
tV=tCK-(d1+d2)
td1
td1
10A
A
13...INPUT BUFFER
16...EXTERNAL CLOCK
14...CLOCK DRIVER
B
17...INTERNAL CLOCK
15...INPUT BUFFER DUMMY
D
S
R
1/2 FREQUENCY DIVIDER
24
1/2 FREQUENCY DIVIDER
10B
11;DELAY CIRCUIT CHAIN
12;DELAY CIRCUIT CHAIN
11';DELAY CIRCUIT CHAIN
12';DELAY CIRCUIT CHAIN

FIG. 49

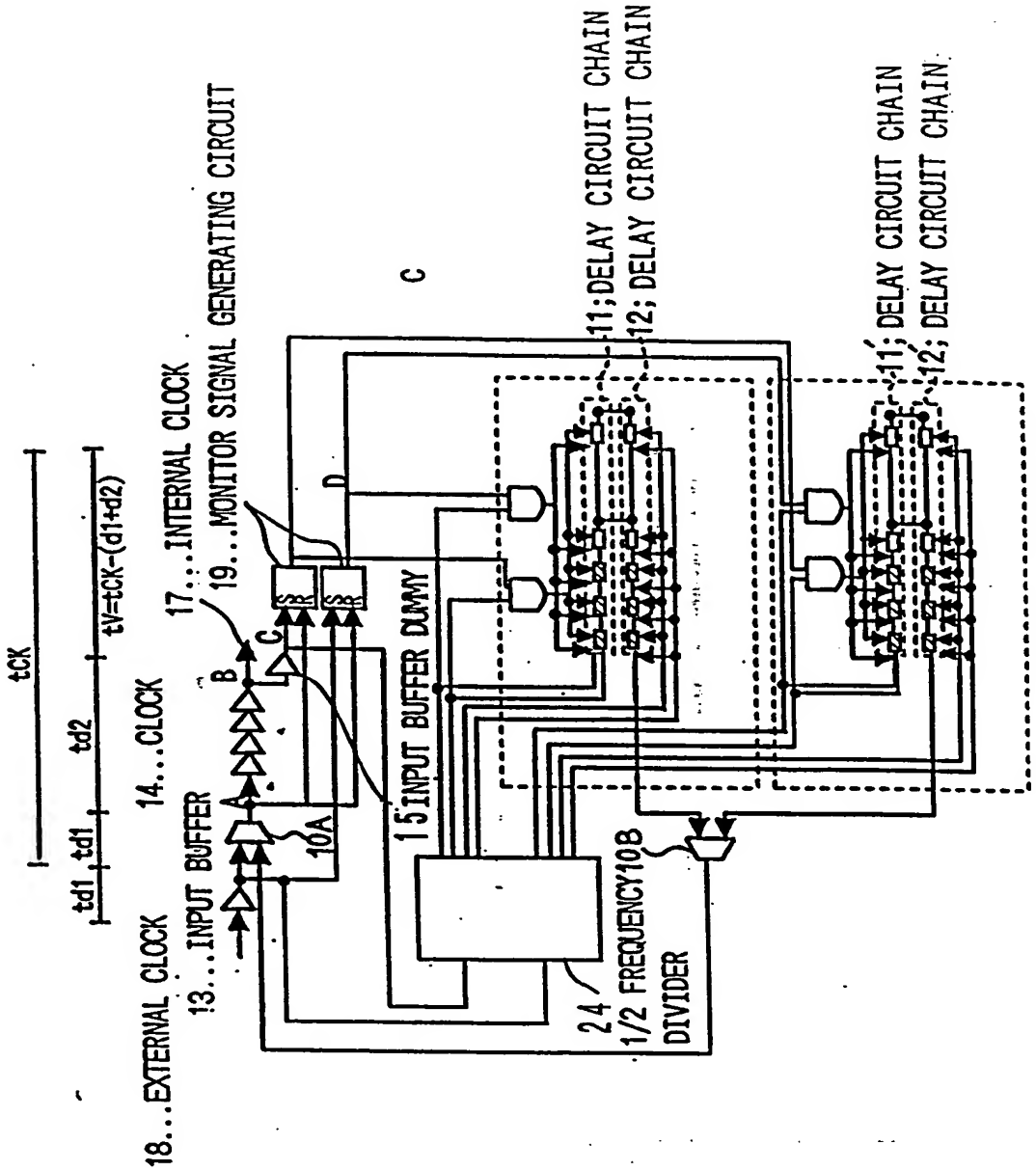

tCK
td1
td2
tV=tCK-(d1+d2)
18...EXTERNAL CLOCK
13...INPUT BUFFER
14...CLOCK
17...INTERNAL CLOCK
19...MONITOR SIGNAL GENERATING CIRCUIT
A
B
C
D
10A
15 INPUT BUFFER DUMMY
11; DELAY CIRCUIT CHAIN
12; DELAY CIRCUIT CHAIN
11'; DELAY CIRCUIT CHAIN
12'; DELAY CIRCUIT CHAIN
24
1/2 FREQUENCY DIVIDER
10B

FIG. 50

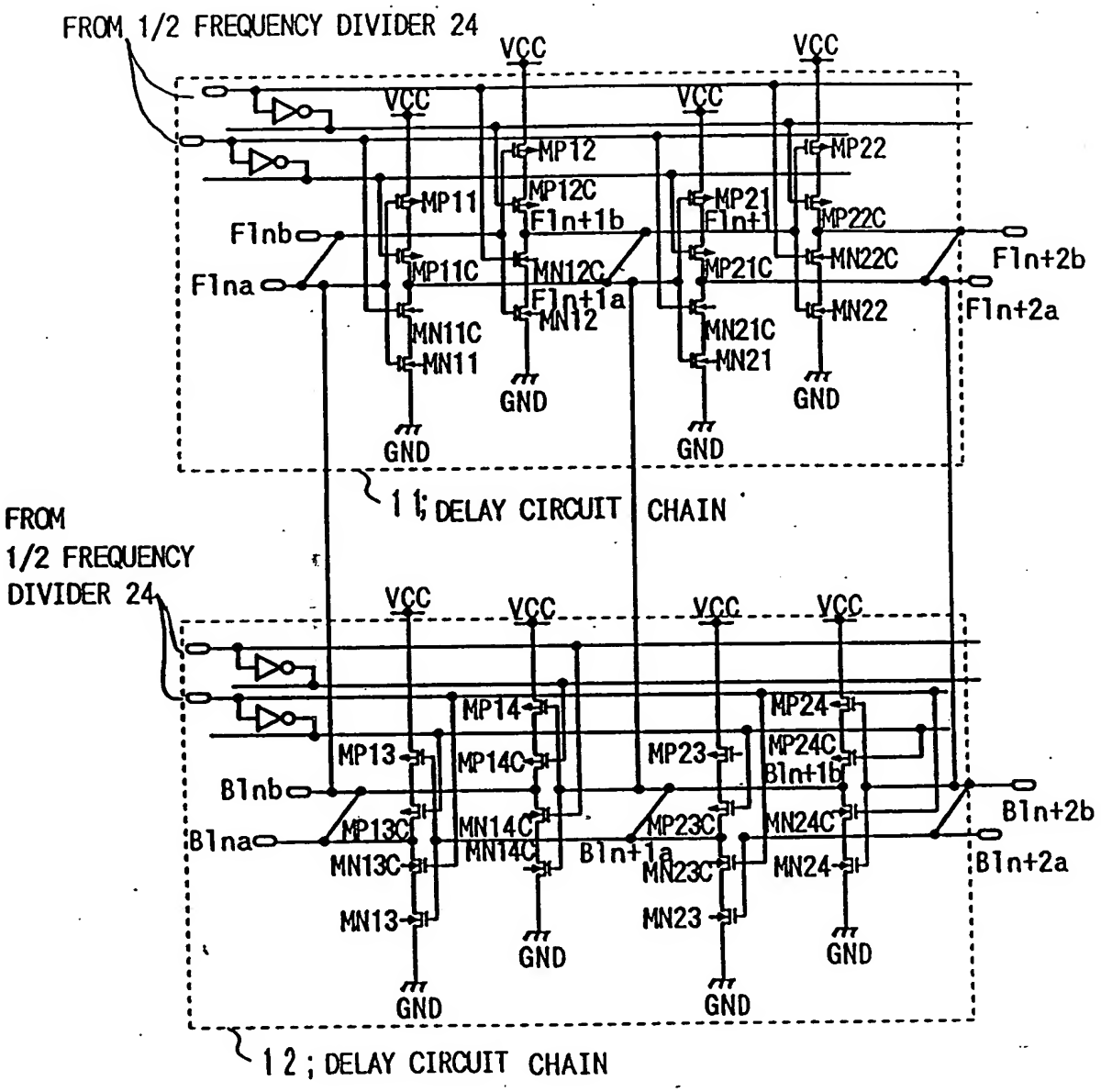
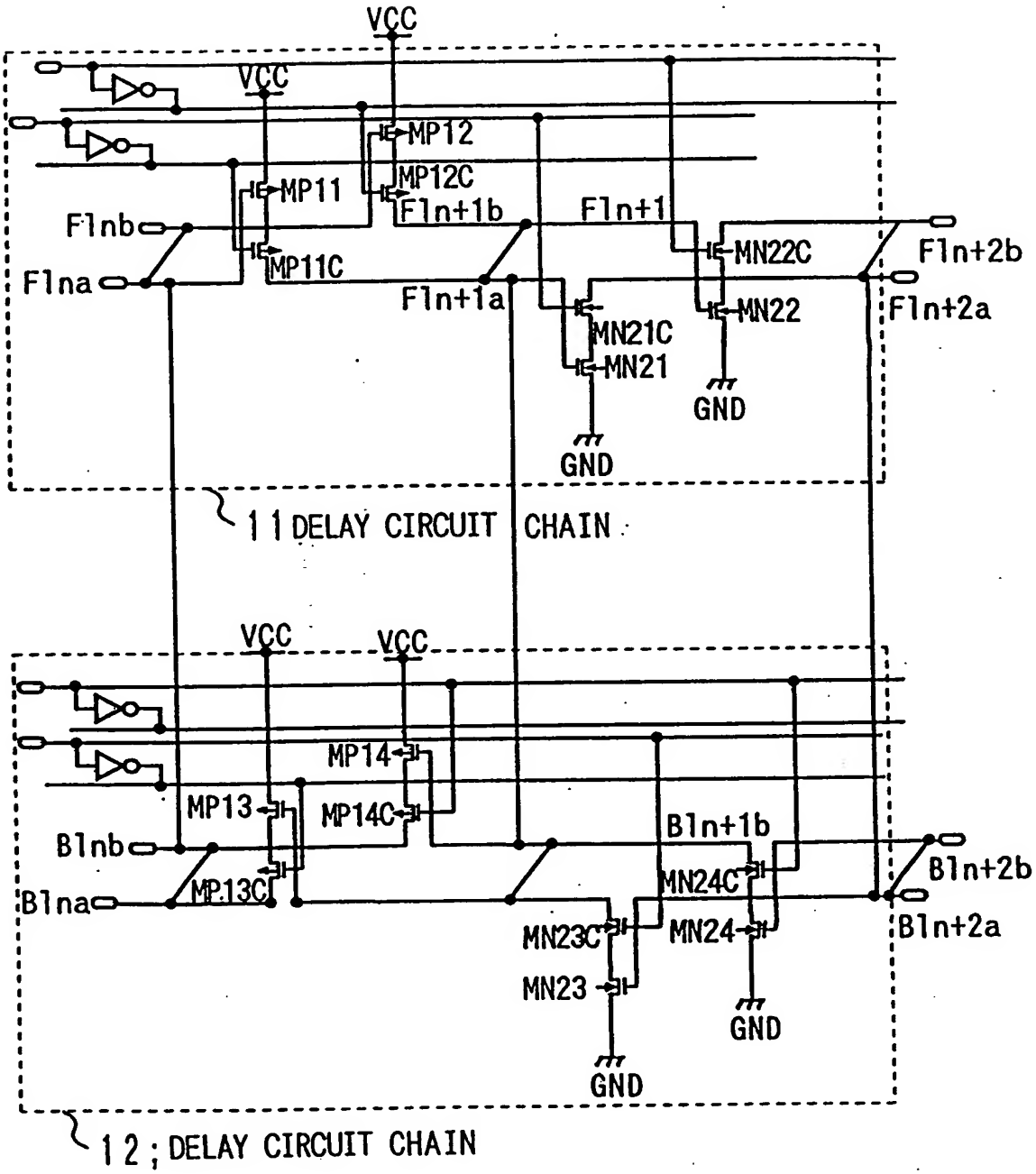

FROM 1/2 FREQUENCY DIVIDER 24
VCC
MP12
MP22
MP11
MP12C
MP21
Fln+1b
Fln+1
MP22C
Flnb
MP11C
MN12C
MP21C
MN22C
Fln+2b
Flna
Fln+1a
MN12
MN22
Fln+2a
MN11C
MN21C
MN11
MN21
GND
11; DELAY CIRCUIT CHAIN
FROM
1/2 FREQUENCY
DIVIDER 24
MP14
MP24
MP13
MP14C
MP23
MP24C
Blnb
Bln+1b
Bln+2b
Blna
MP13C
MN14C
MP23C
MN24C
MN13C
MN14C
Bln+1a
MN23C
MN24
Bln+2a
MN13
MN23
12; DELAY CIRCUIT CHAIN

FIG. 51


VCC
VCC
MP12
MP11
MP12C
Fln+1b
Fln+1
Flnb
MP11C
MN22C
Fln+2b
Flna
Fln+1a
MN22
Fln+2a
MN21C
MN21
GND
GND
11 DELAY CIRCUIT CHAIN
VCC
VCC
MP14
MP13
MP14C
Bln+1b
Blnb
MP13C
MN24C
Bln+2b
Blna
MN23C
MN24
Bln+2a
MN23
GND
GND
12 ; DELAY CIRCUIT CHAIN

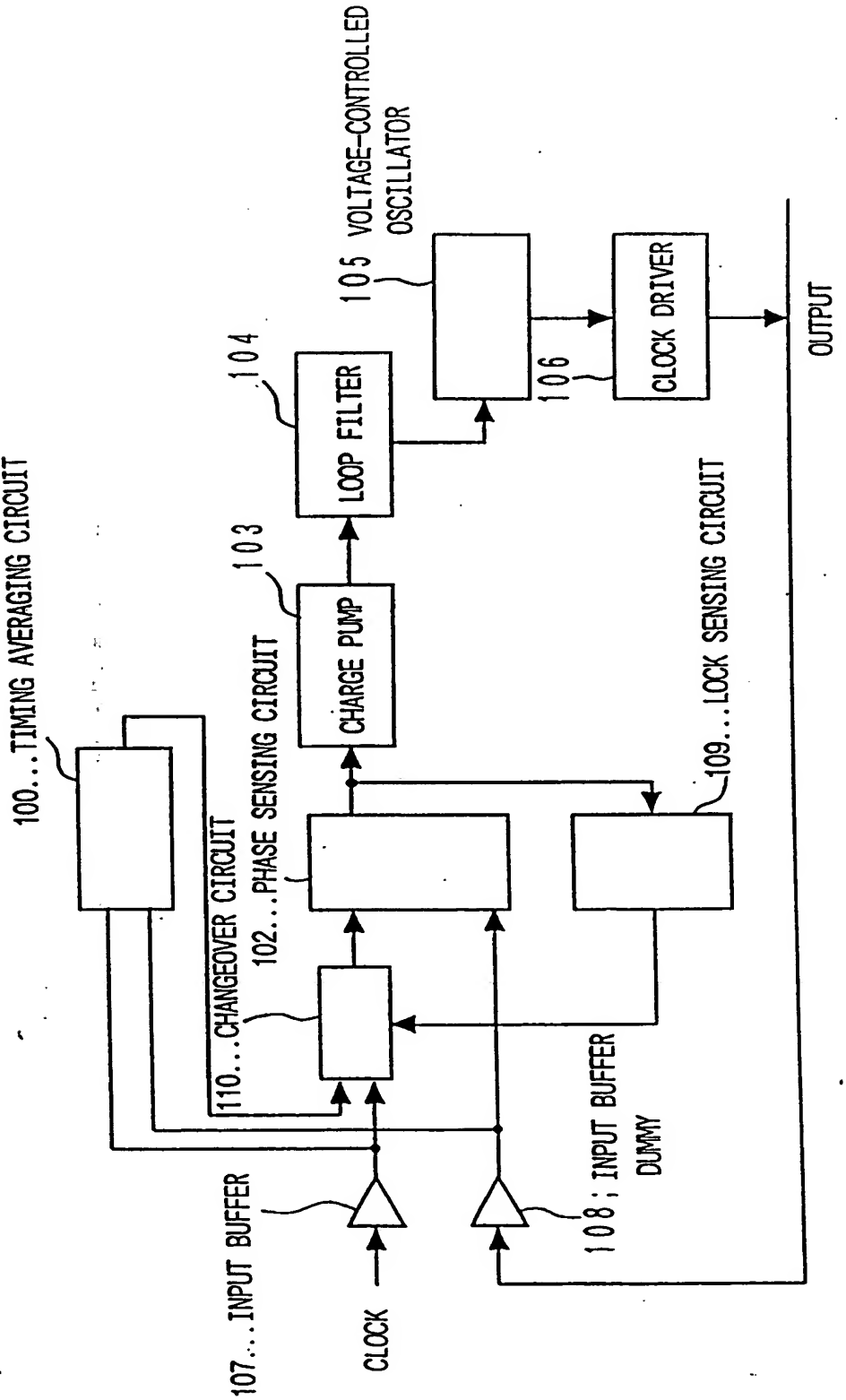

100...TIMING AVERAGING CIRCUIT
110...CHANGEOVER CIRCUIT
102...PHASE SENSING CIRCUIT
103
CHARGE PUMP
104
LOOP FILTER
105 VOLTAGE-CONTROLLED OSCILLATOR
106
CLOCK DRIVER
OUTPUT
109...LOCK SENSING CIRCUIT
107...INPUT BUFFER
CLOCK
108; INPUT BUFFER DUMMY

FIG. 52